

Gemini Complex Corporation

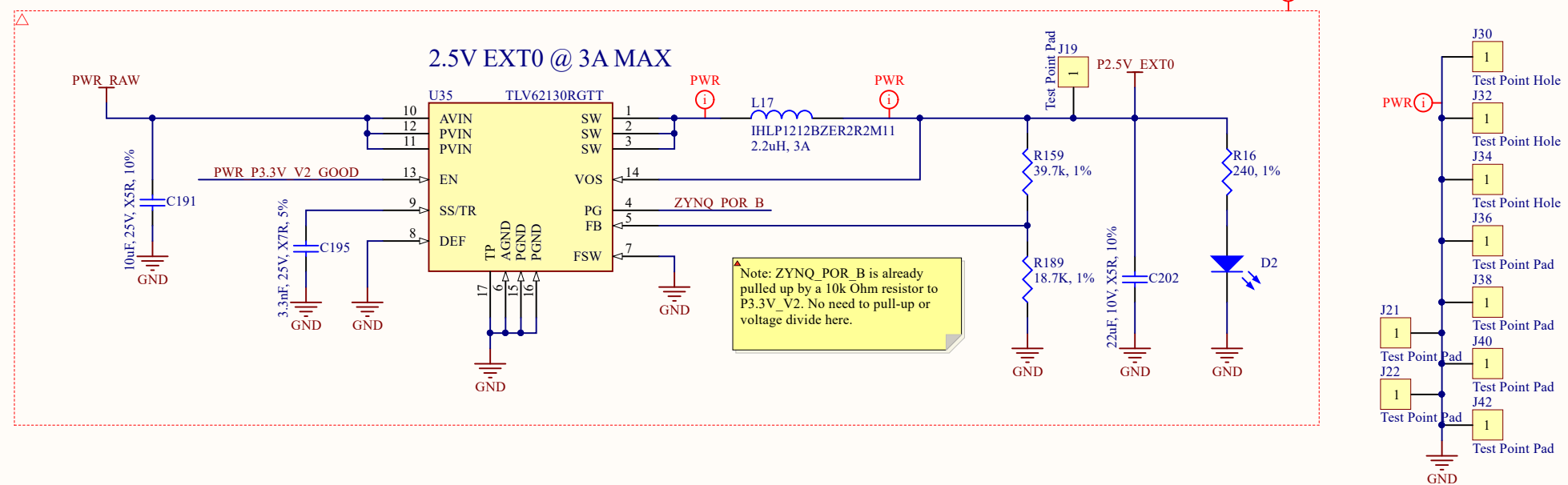
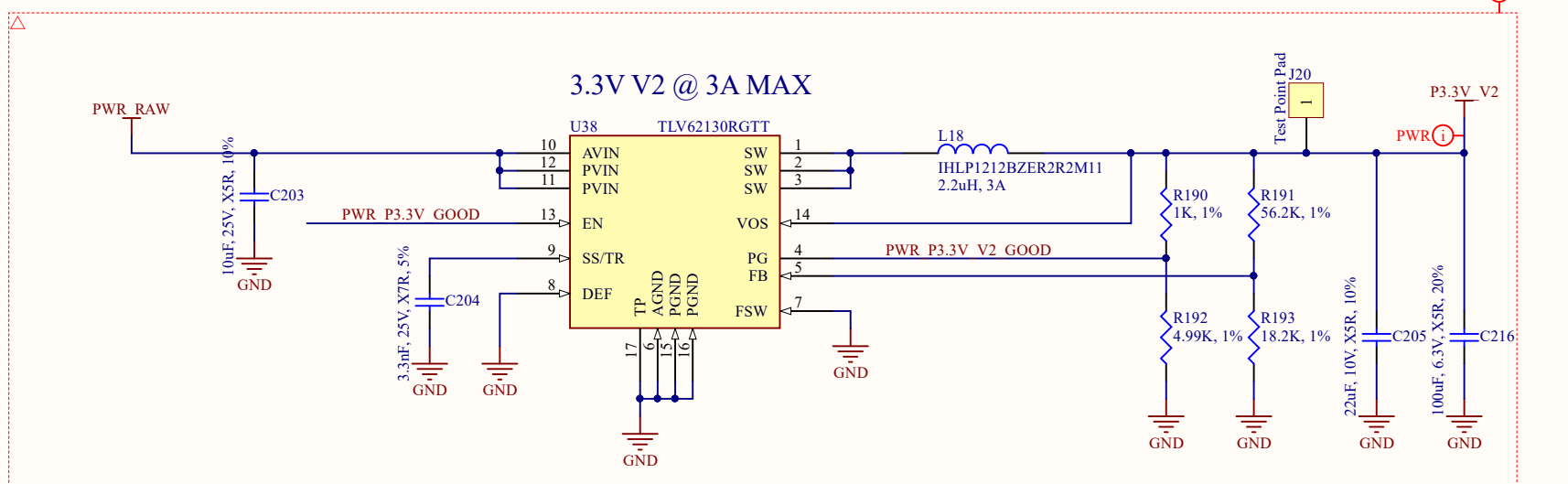
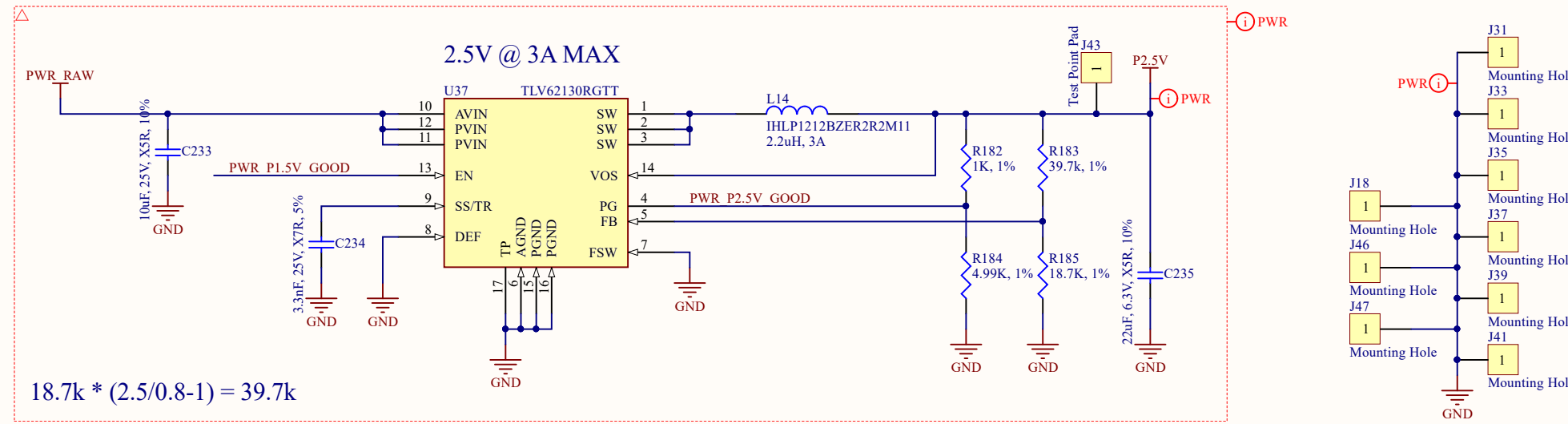
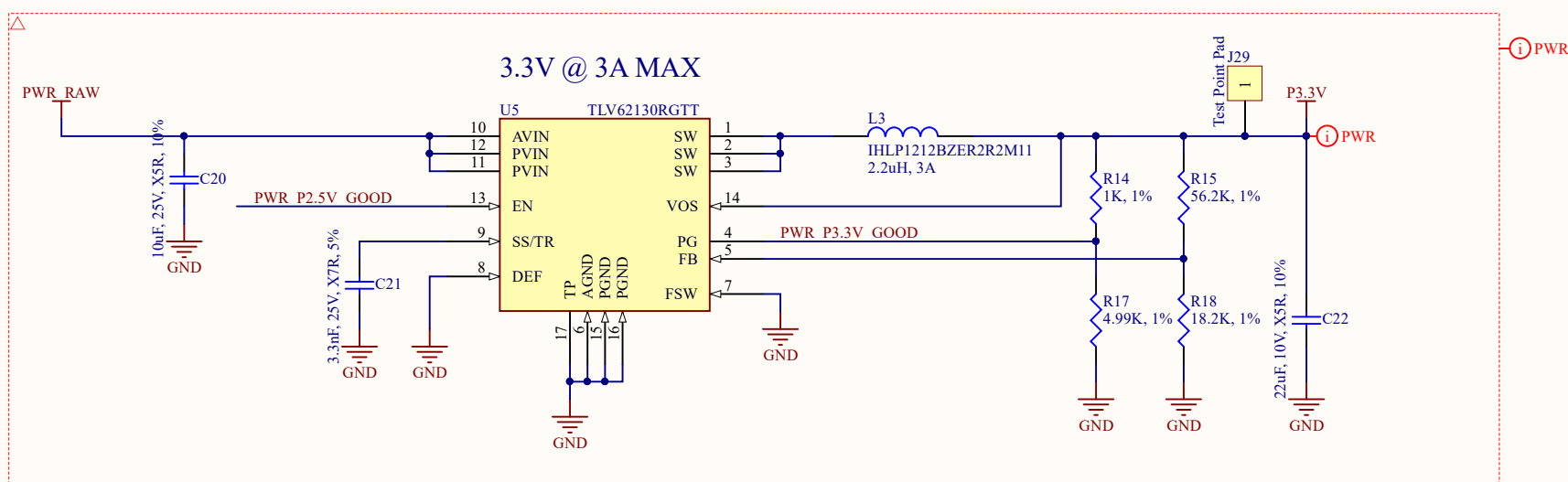
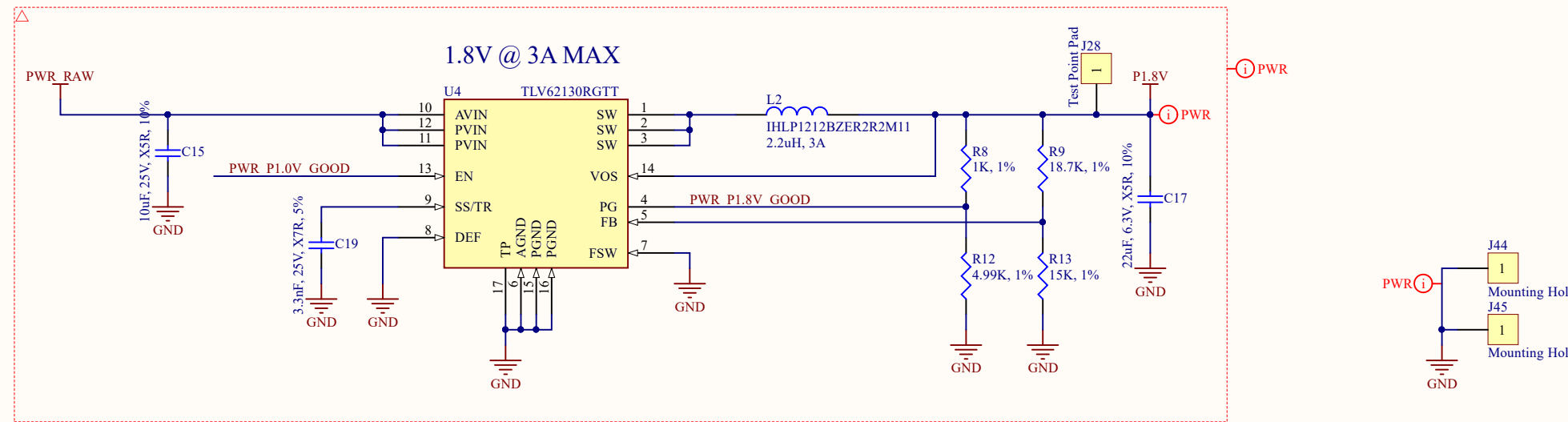
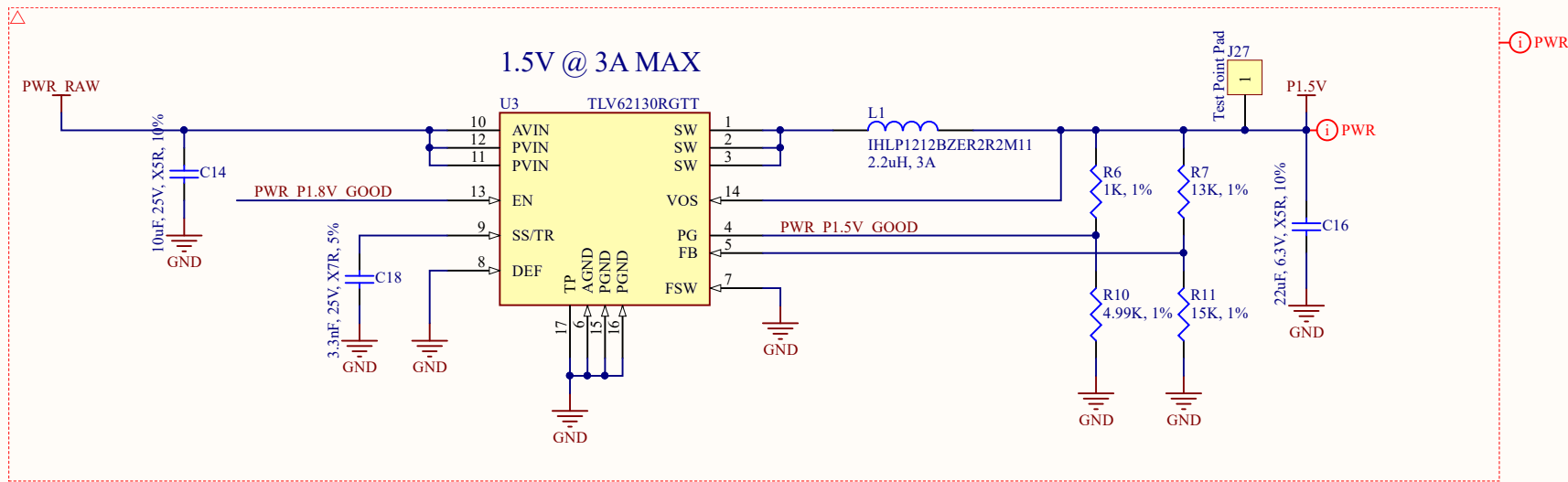
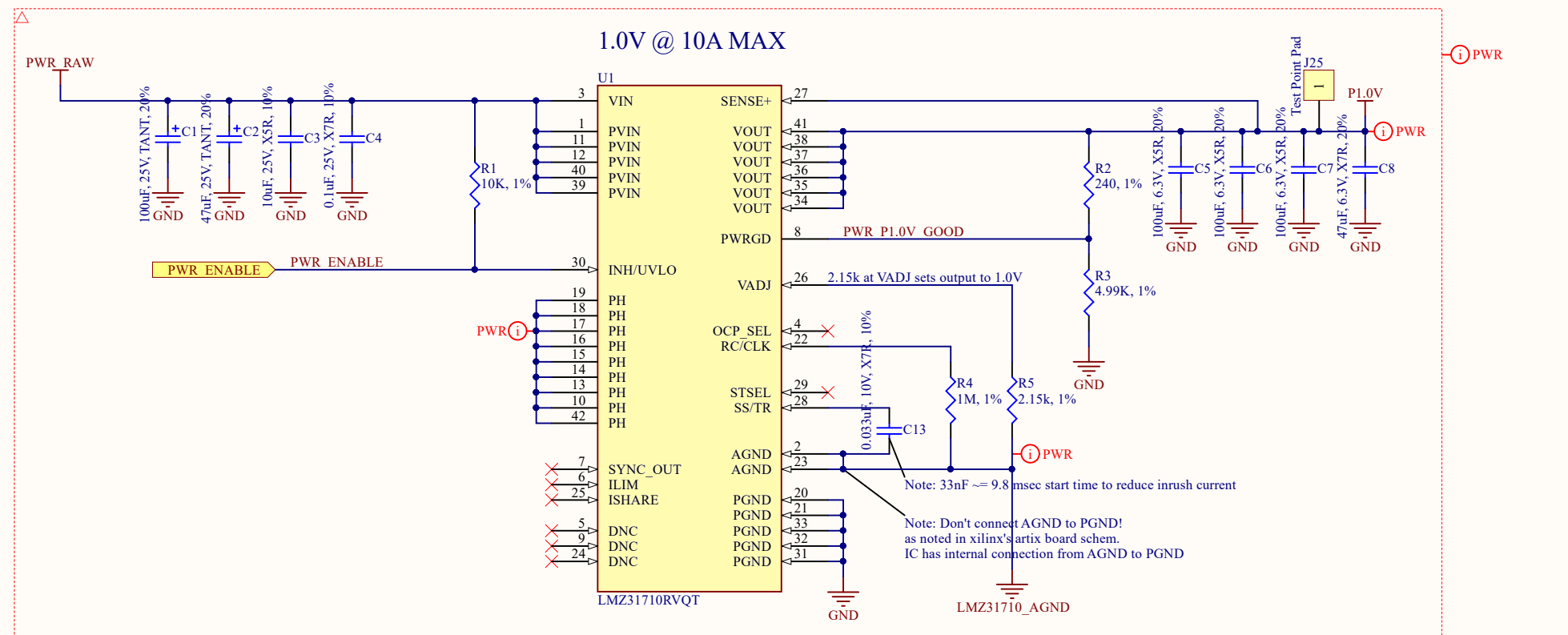
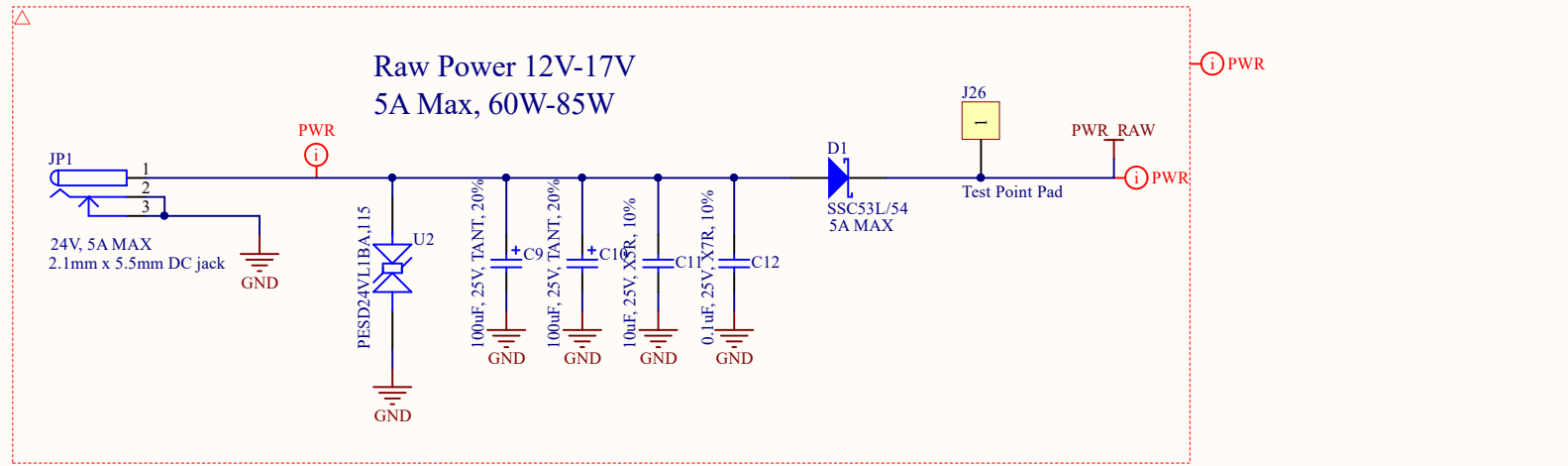
Gemini Prototype Mk.I Rev 2

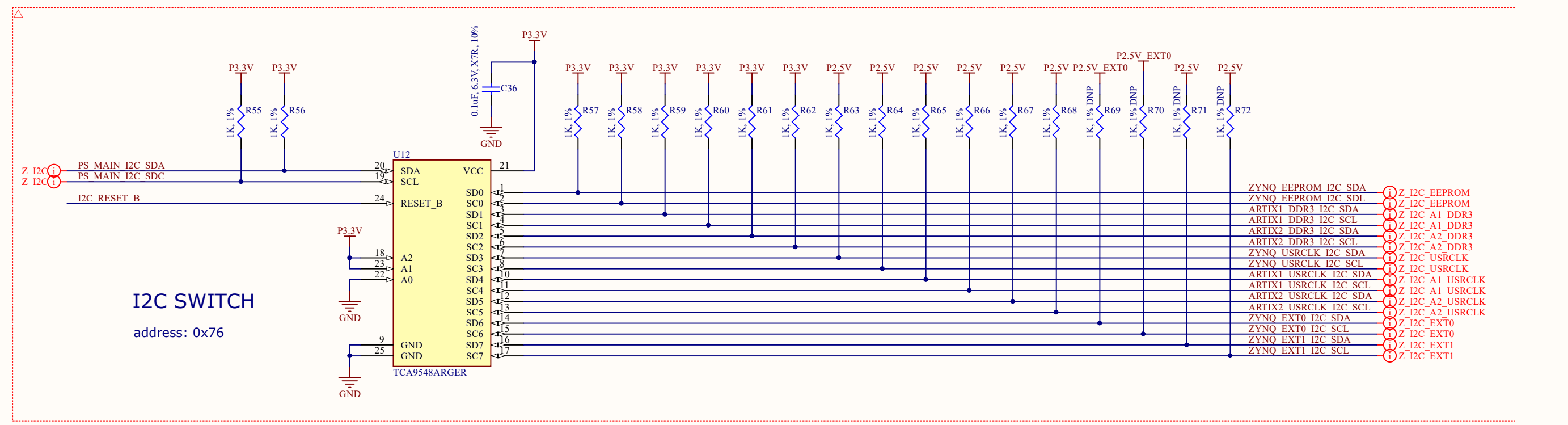
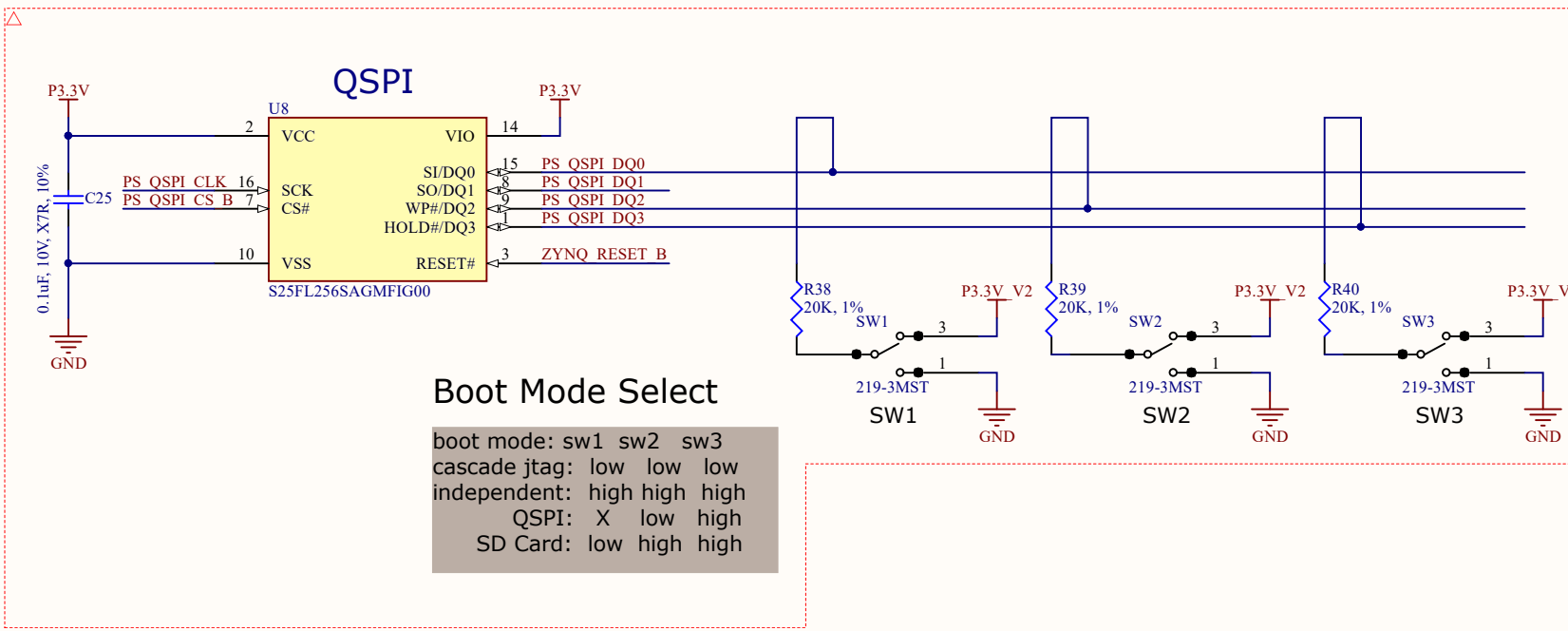
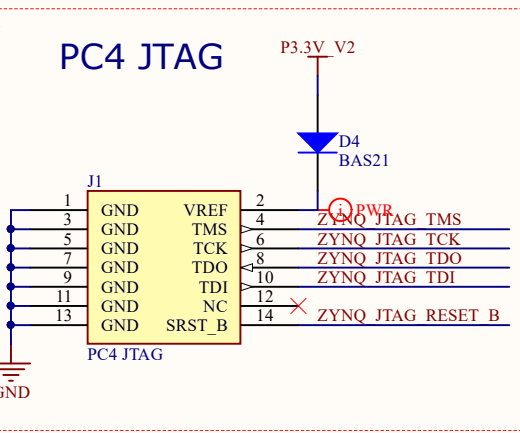
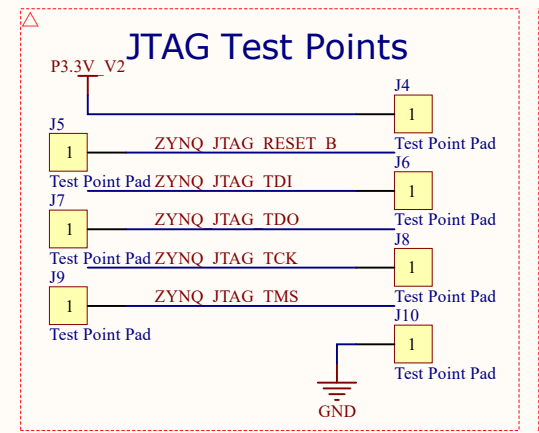
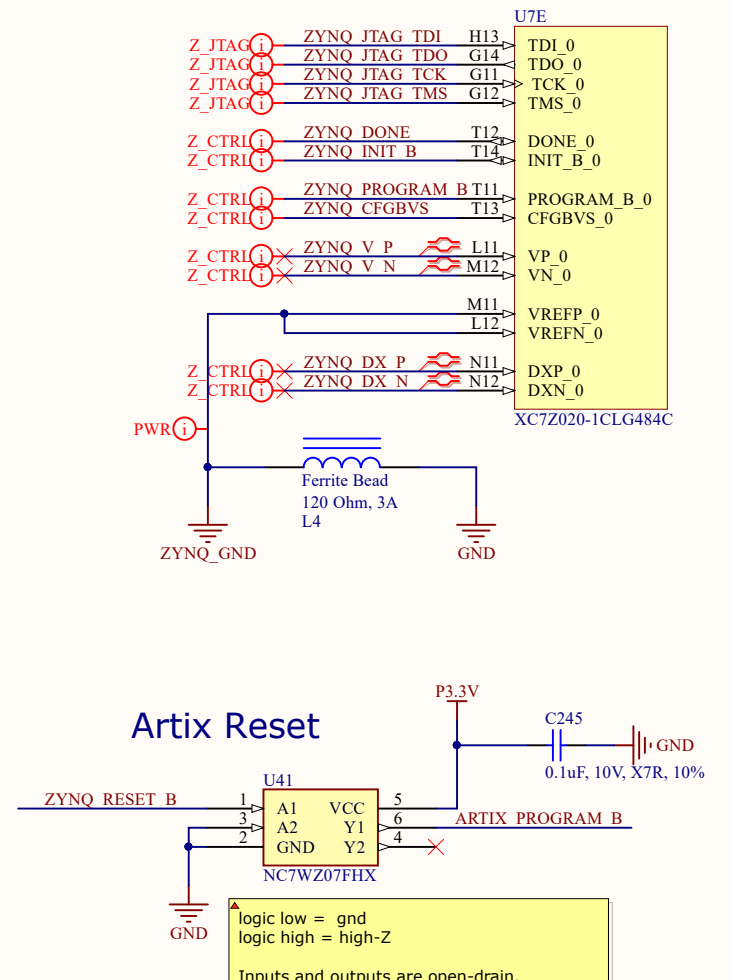
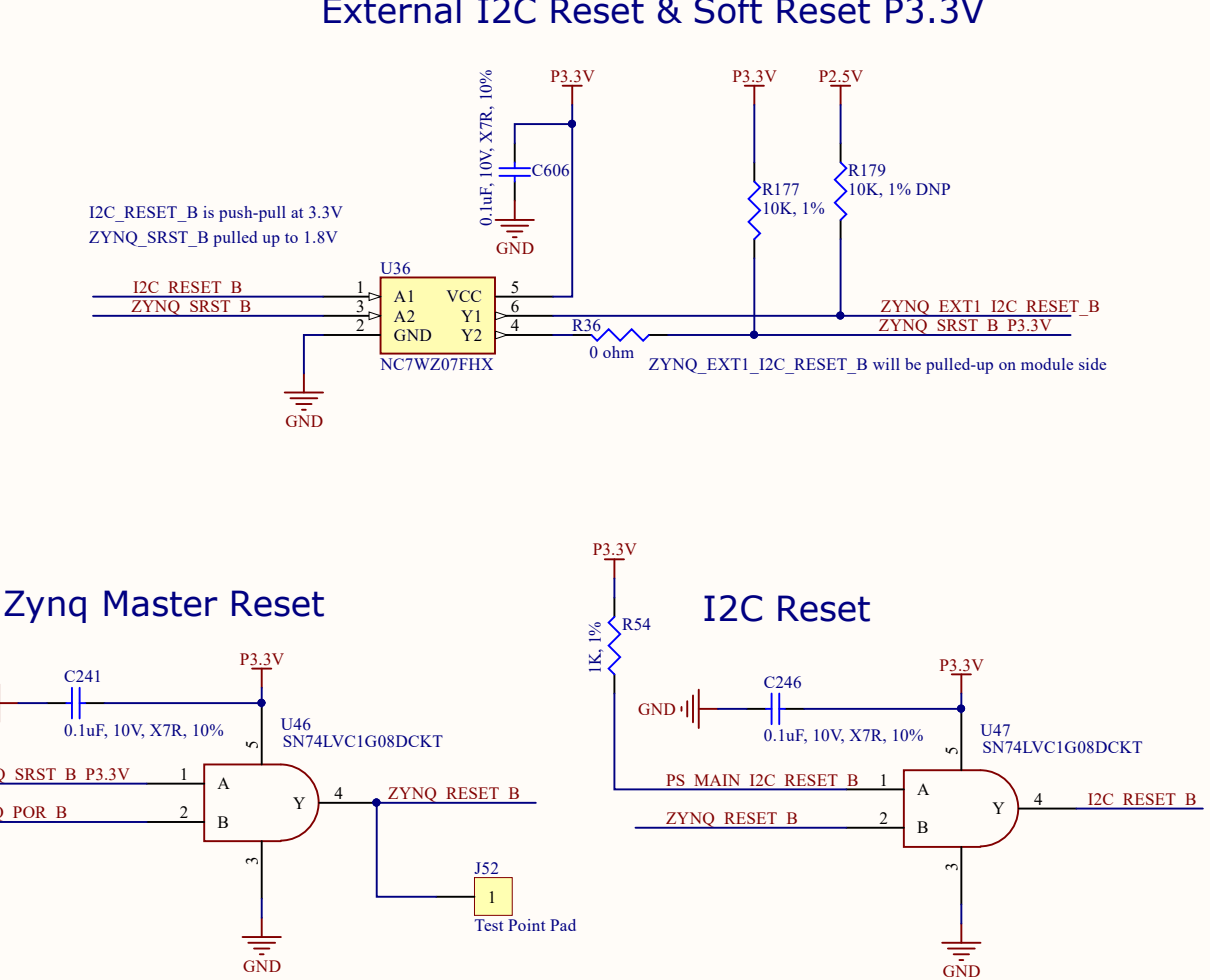
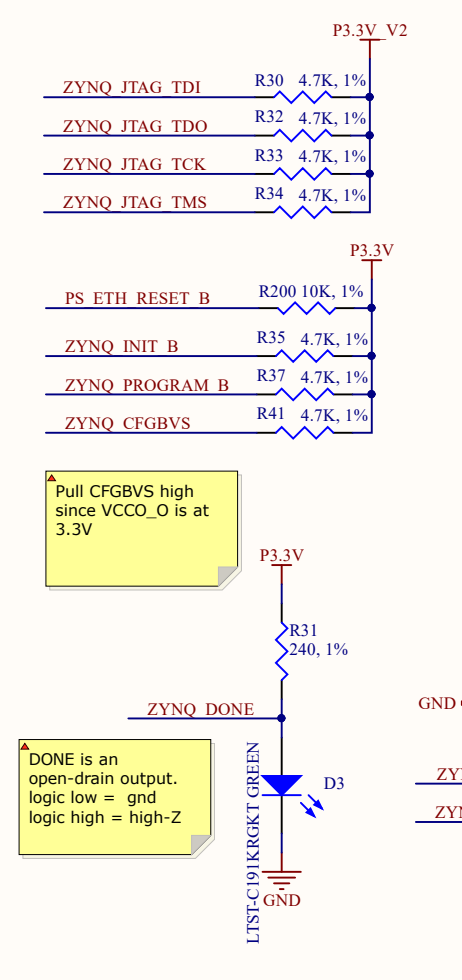
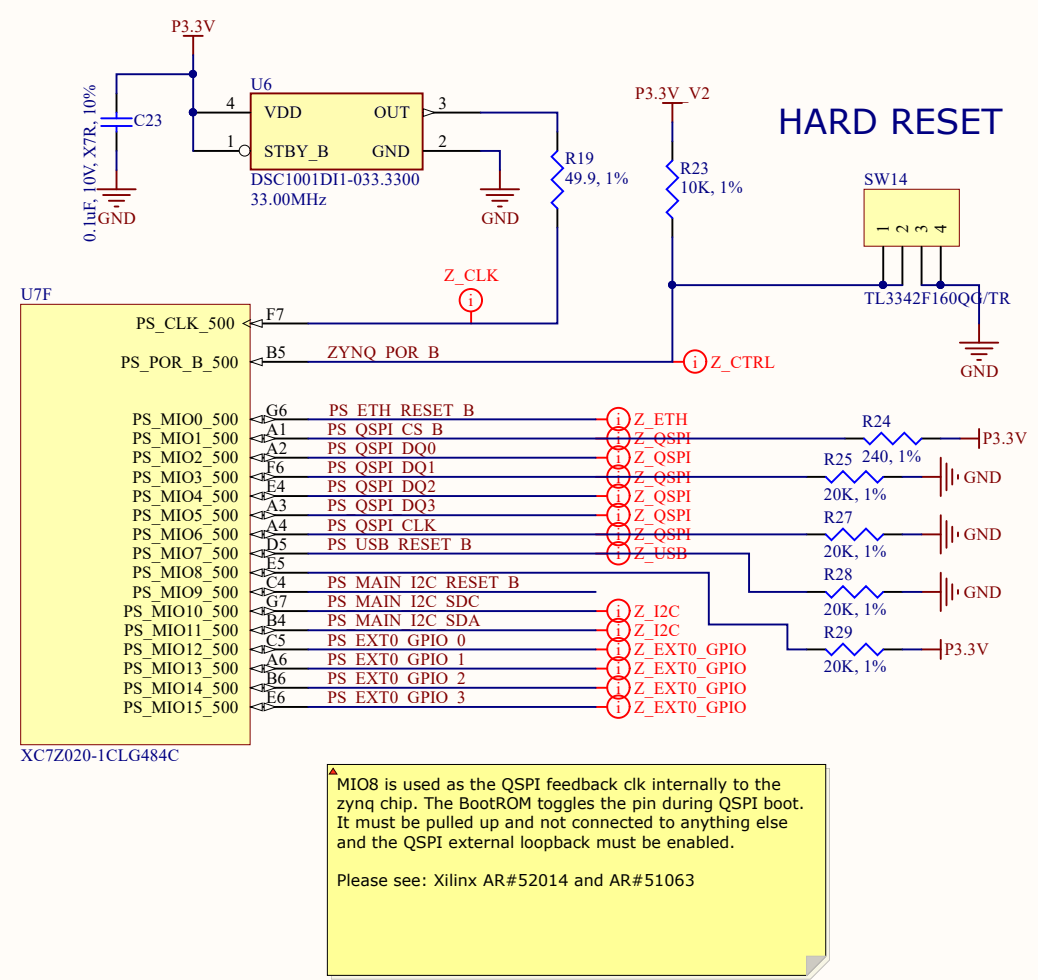
5/2018

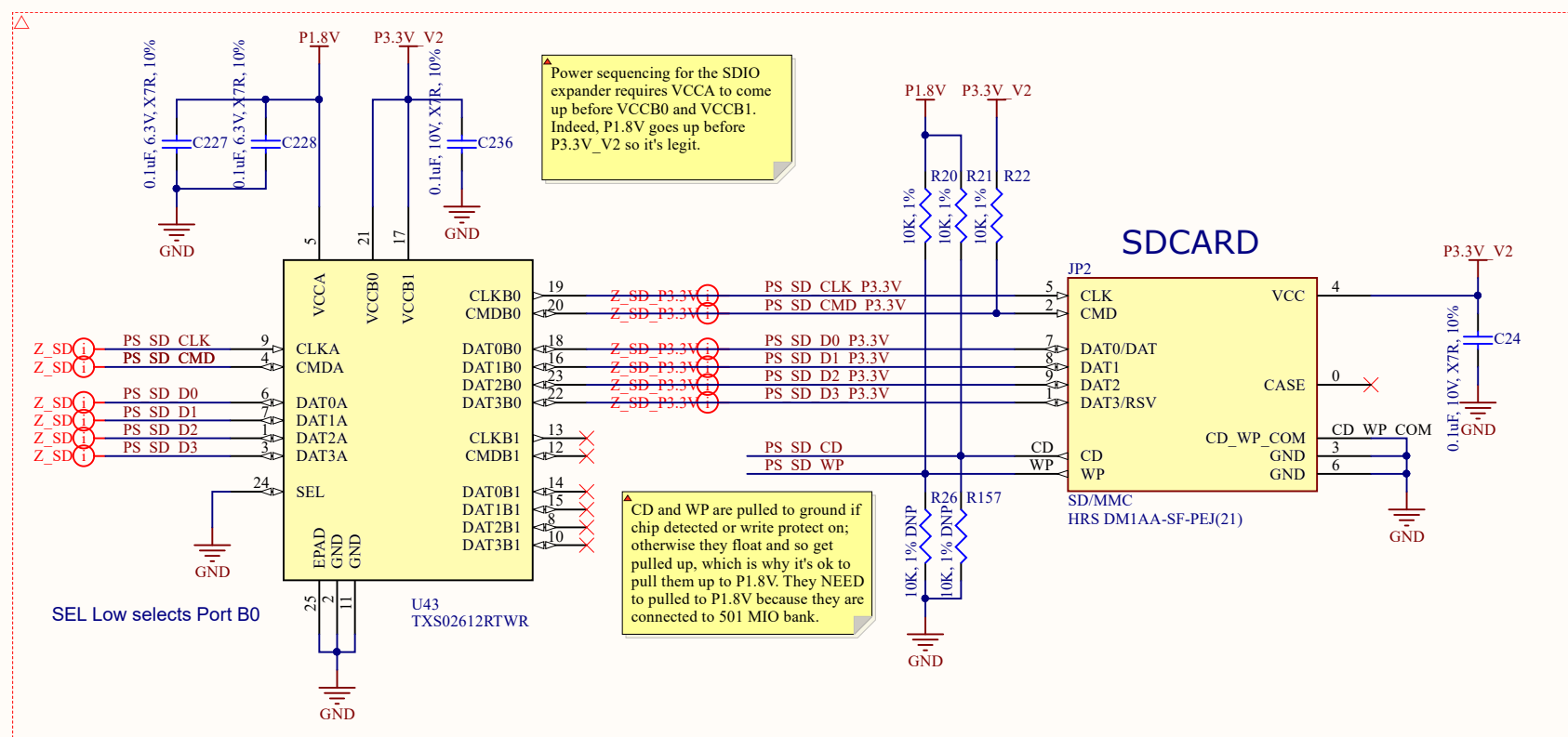
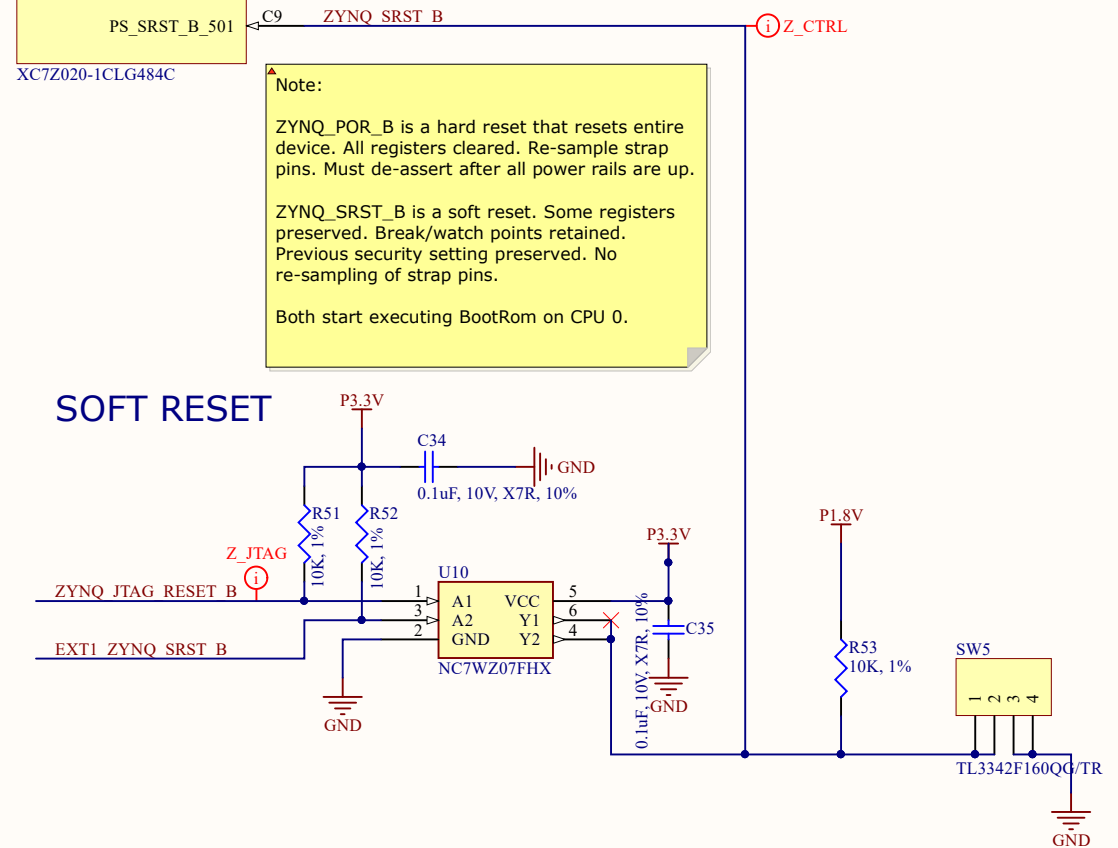
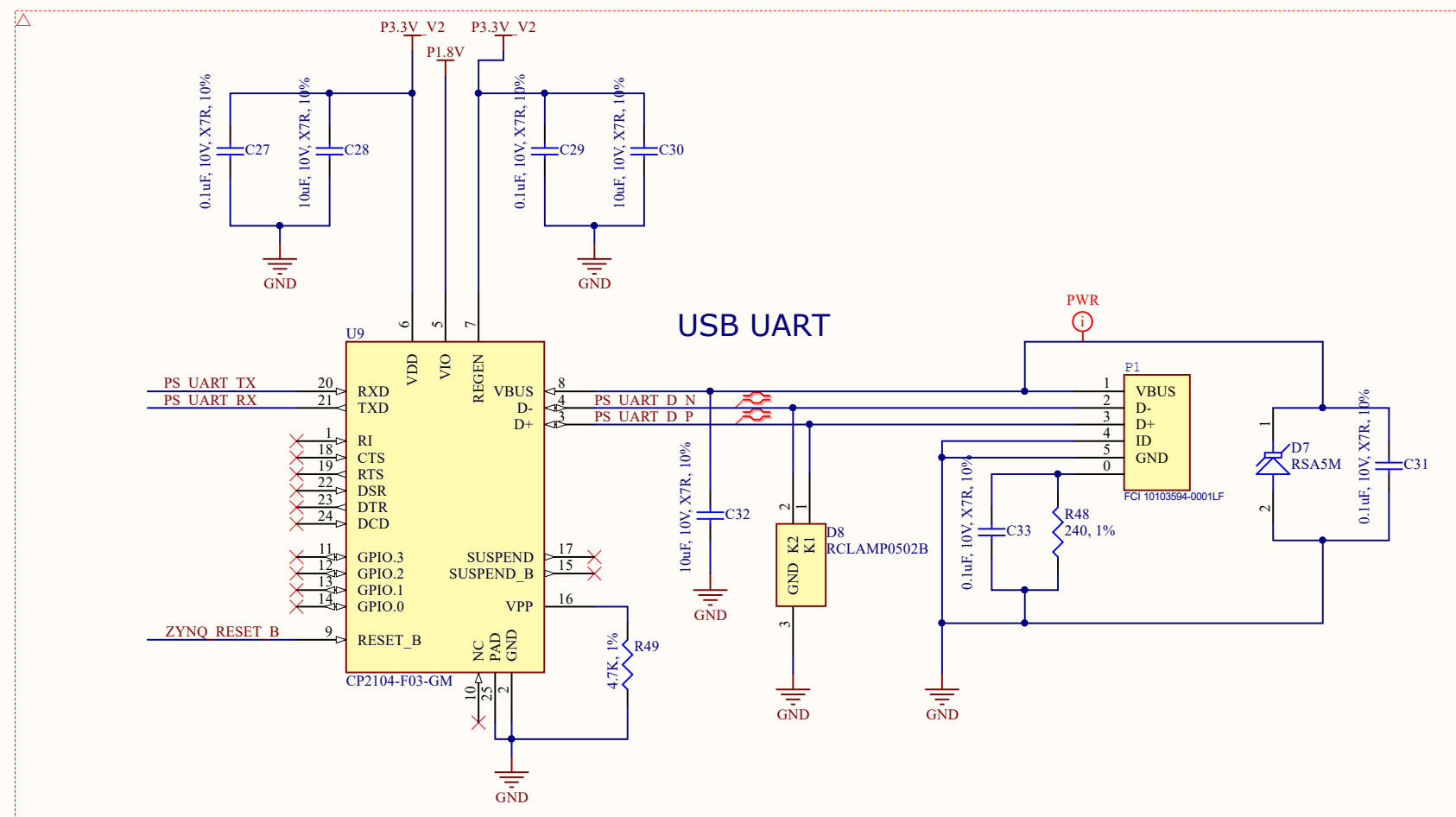
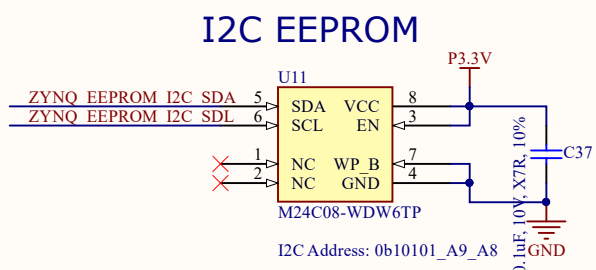
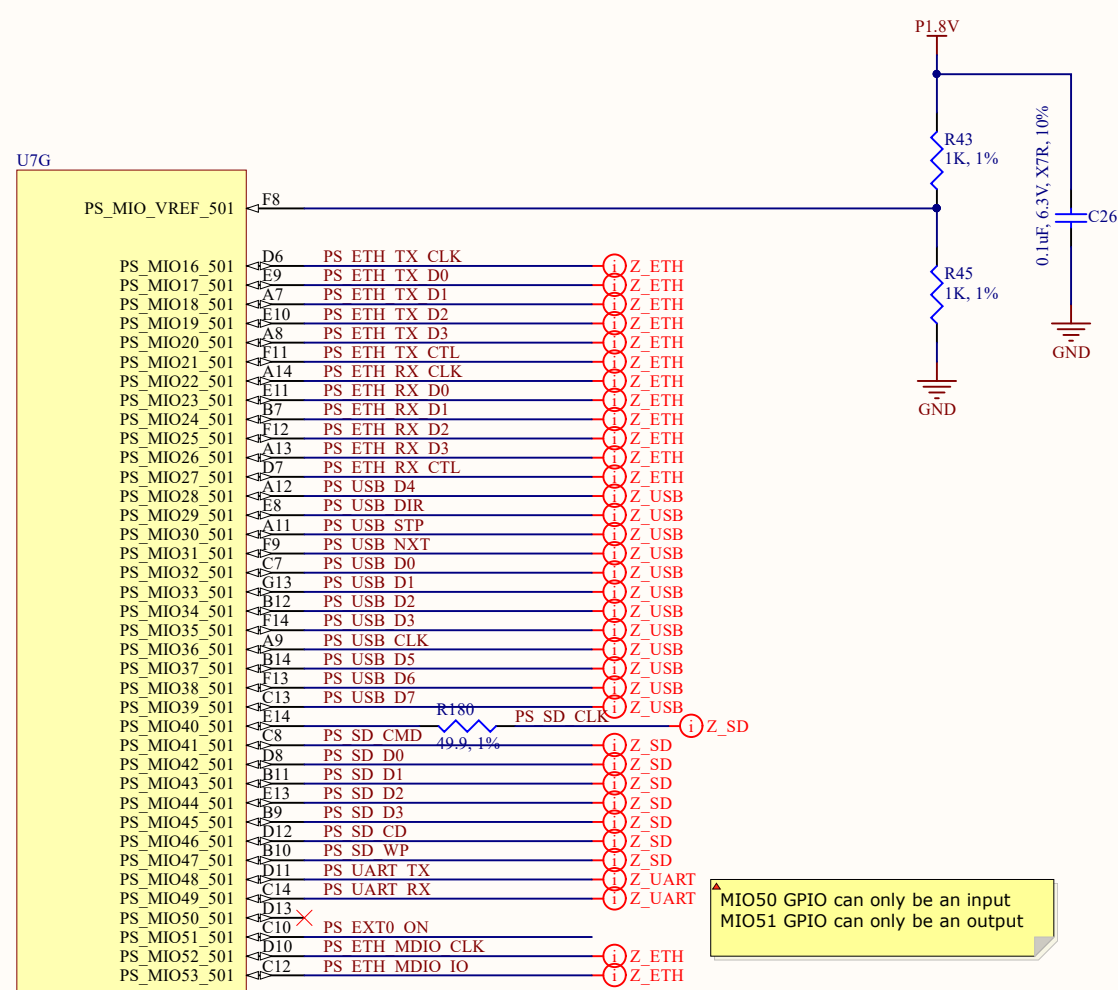
- 01 - Power
- 02 - Zynq
- 03 - Zynq MIO & UART, SD, I2C
- 04 - Zynq IO & EXT0
- 05 - Zynq DDR3 Memory
- 06 - Zynq Ethernet & USB
- 07 - Zynq Power
- 08 - Artix1
- 09 - Artix1 IO
- 10 - Artix1 DDR3 Memory
- 11 - Artix1 Power
- 12 - Artix2
- 13 - Artix2 IO
- 14 - Artix2 DDR3 Memory
- 15 - Artix2 Power
- 16 - EXT1 Expansion



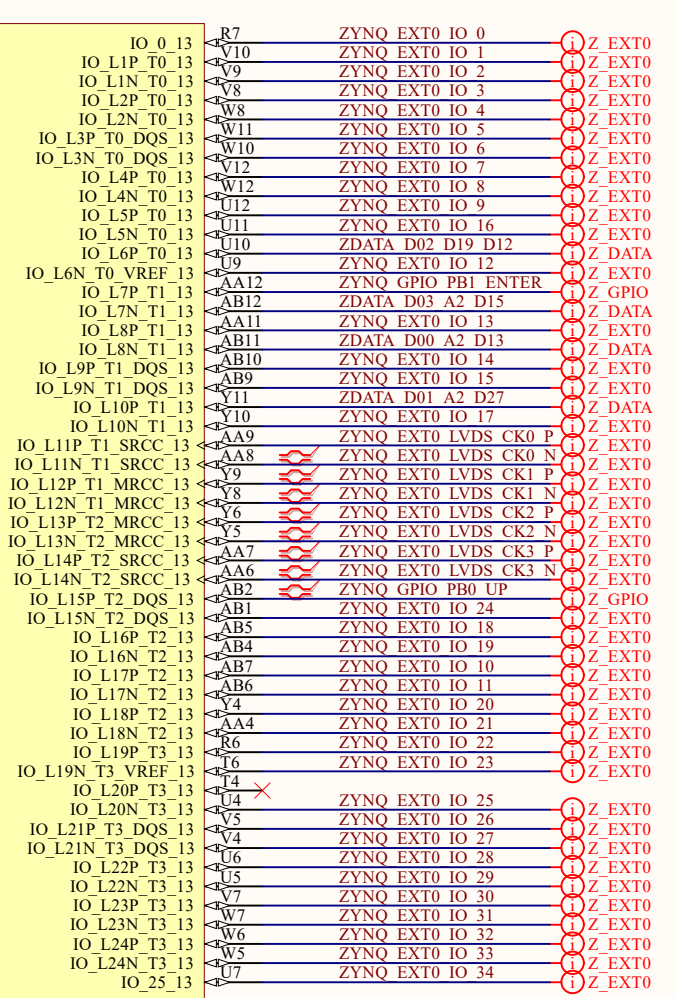
Power Sequence Order: 1.0V -> 1.8V -> 1.5V -> 2.5V -> 3.3V -> 3.3V_V2 -> 2.5V_EXT0





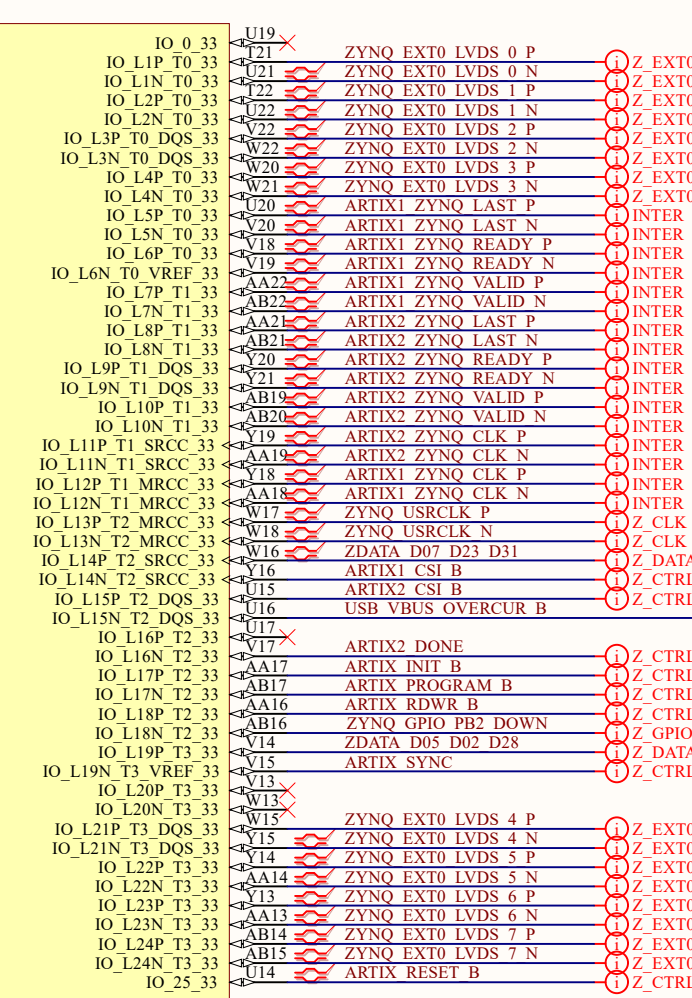


U7A
BANK 13



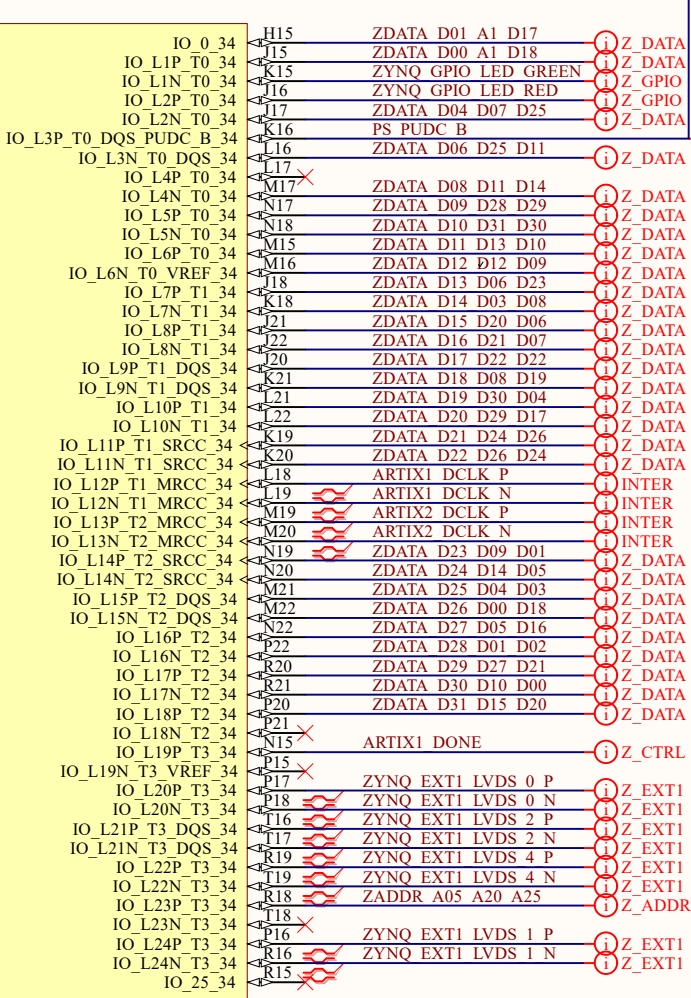
XC7Z020-1CLG484C

U7B
BANK 33



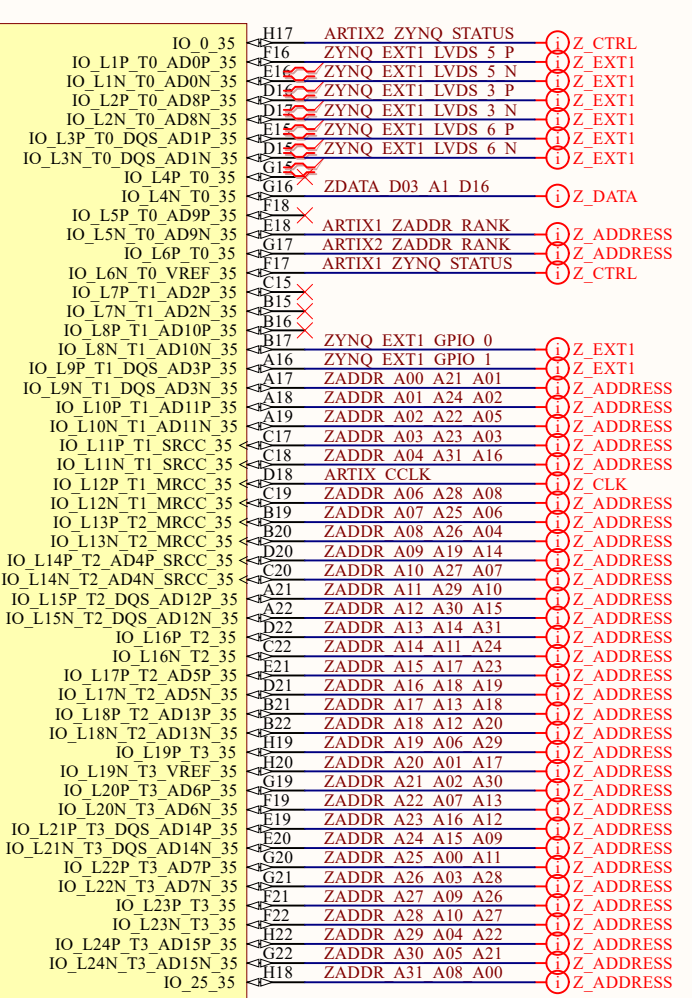
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U7C
BANK 34



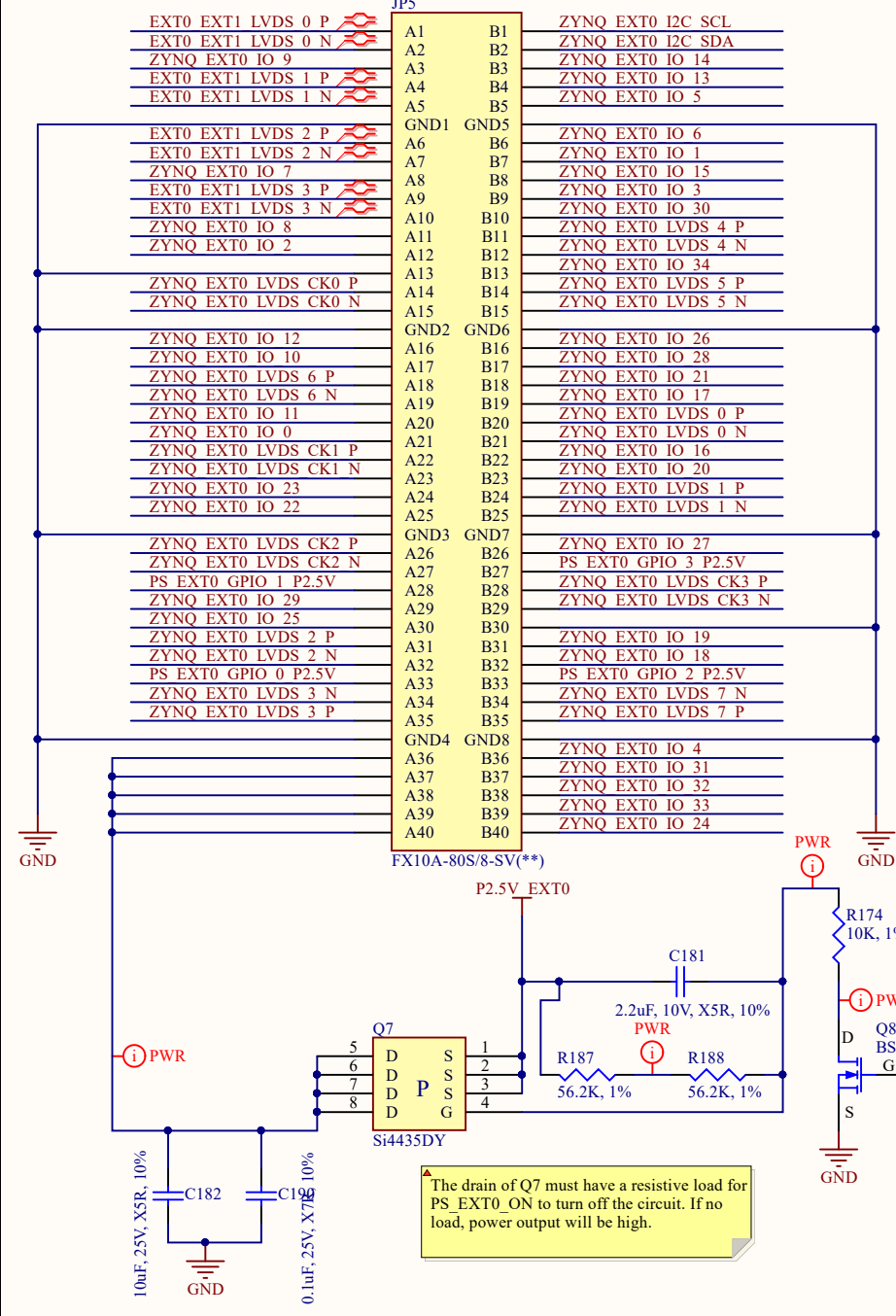
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U7D
BANK 35

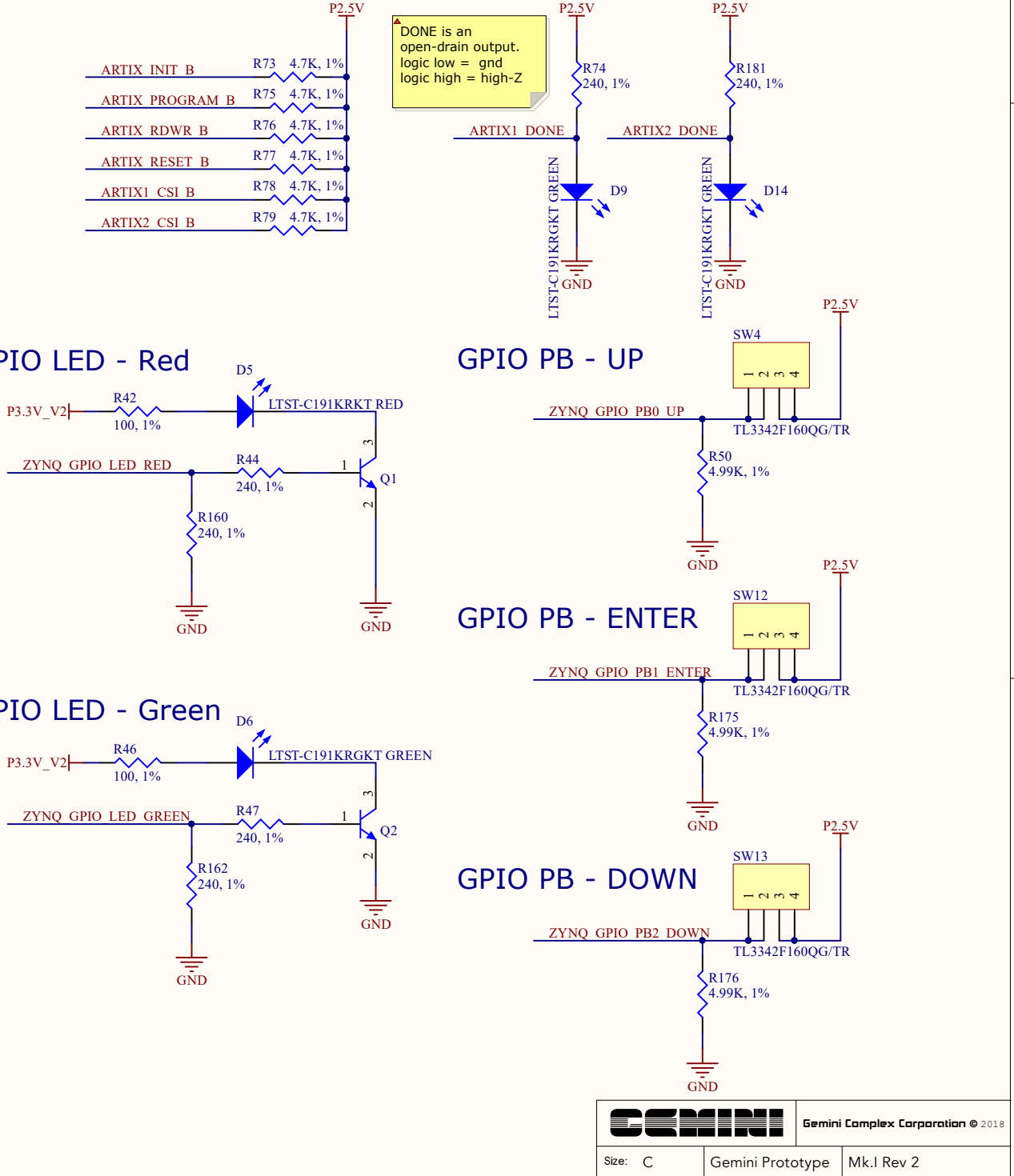
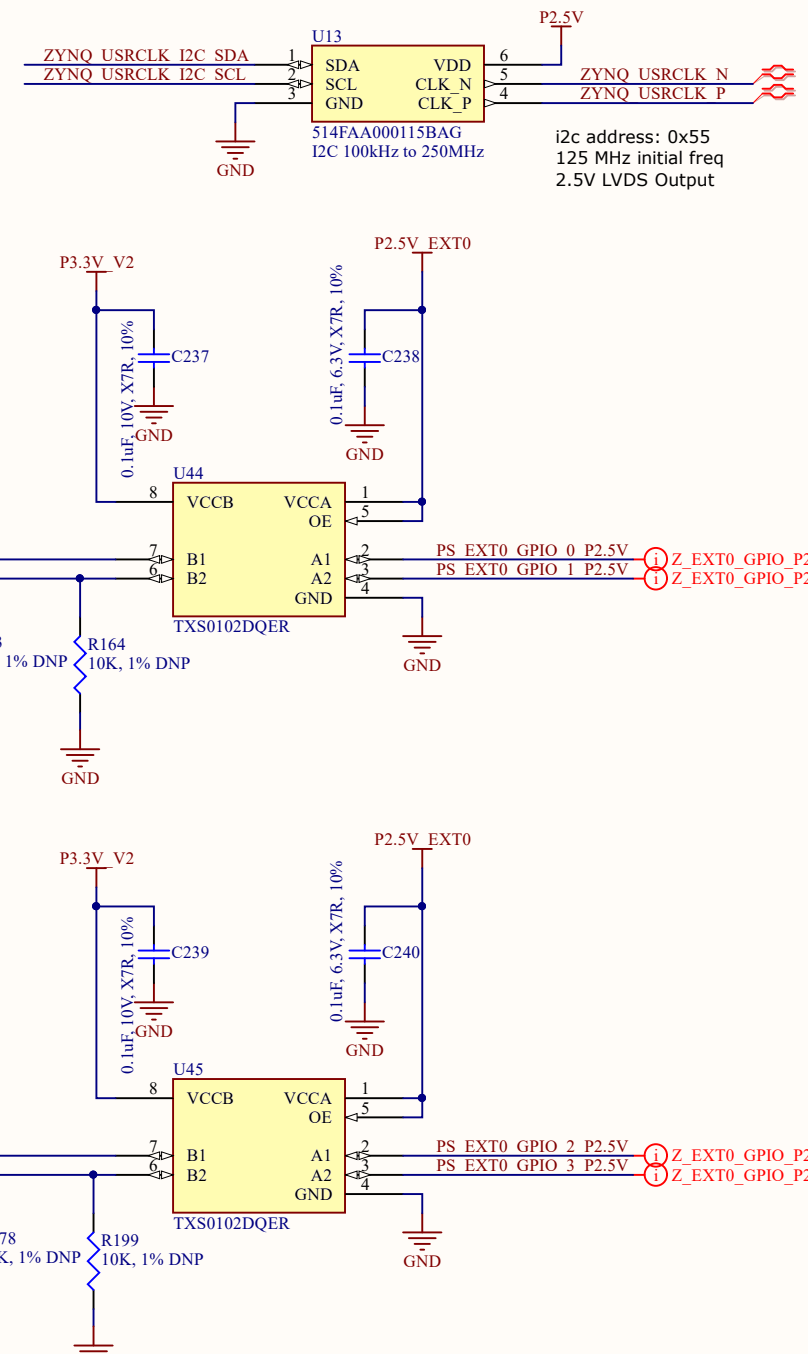


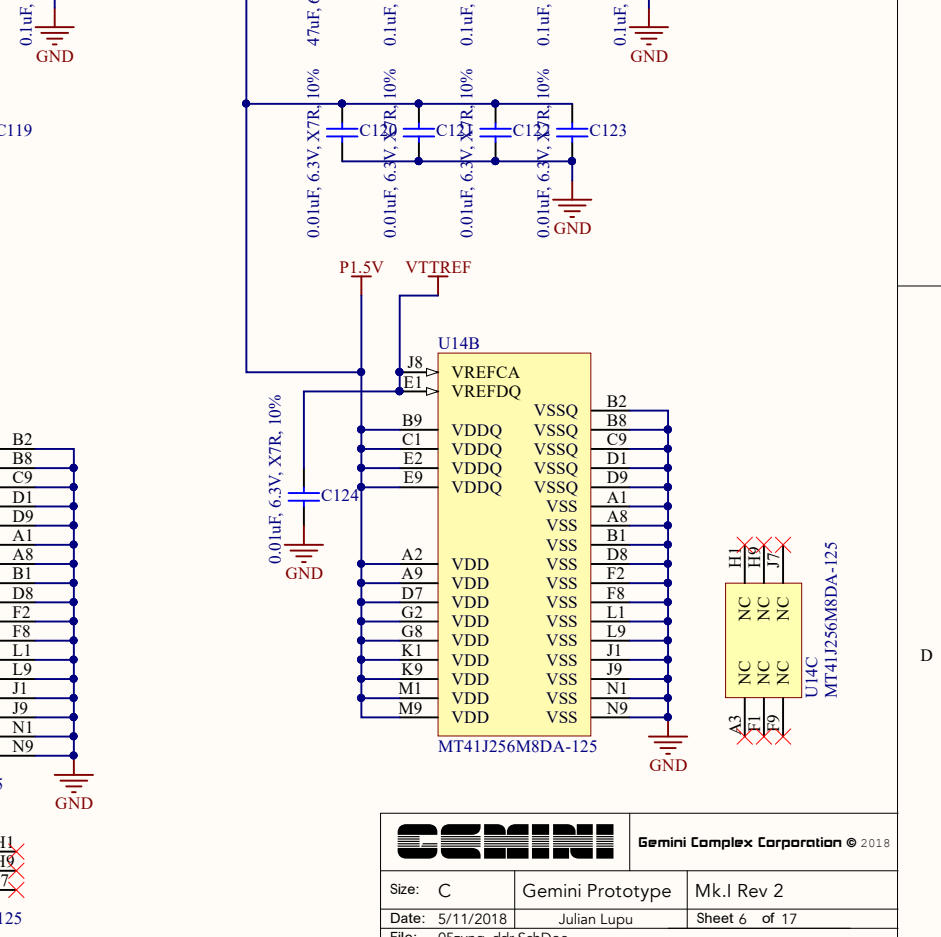
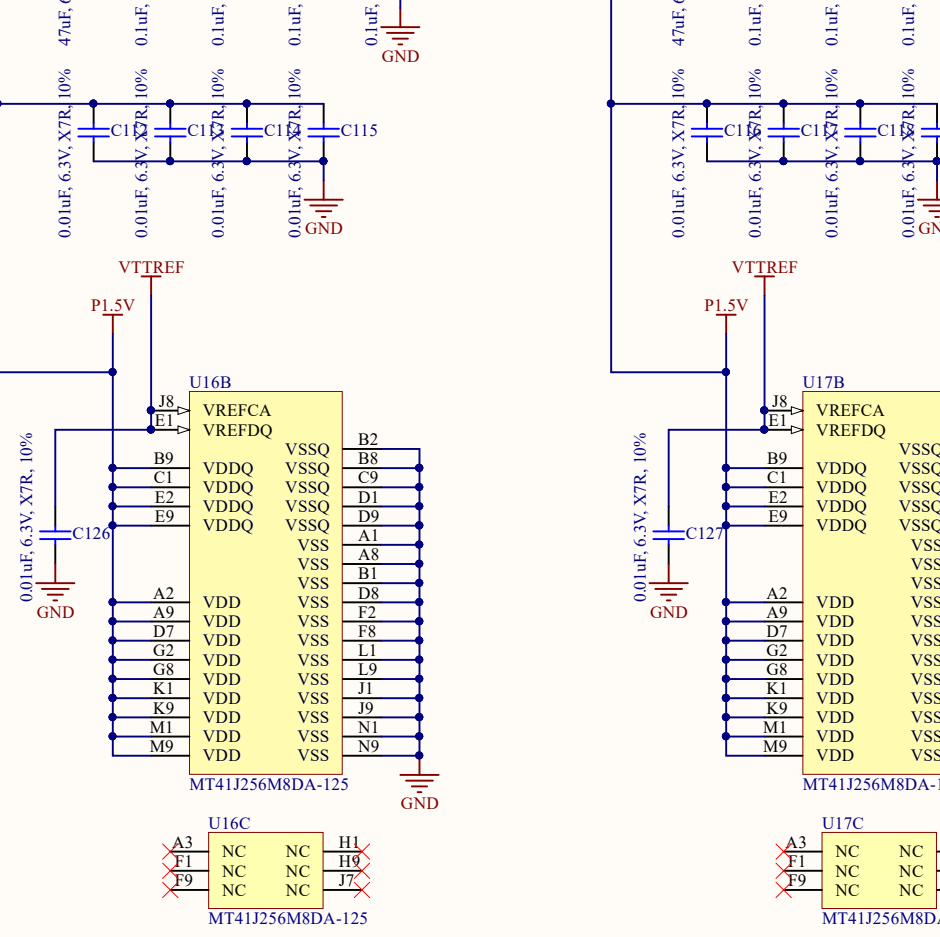
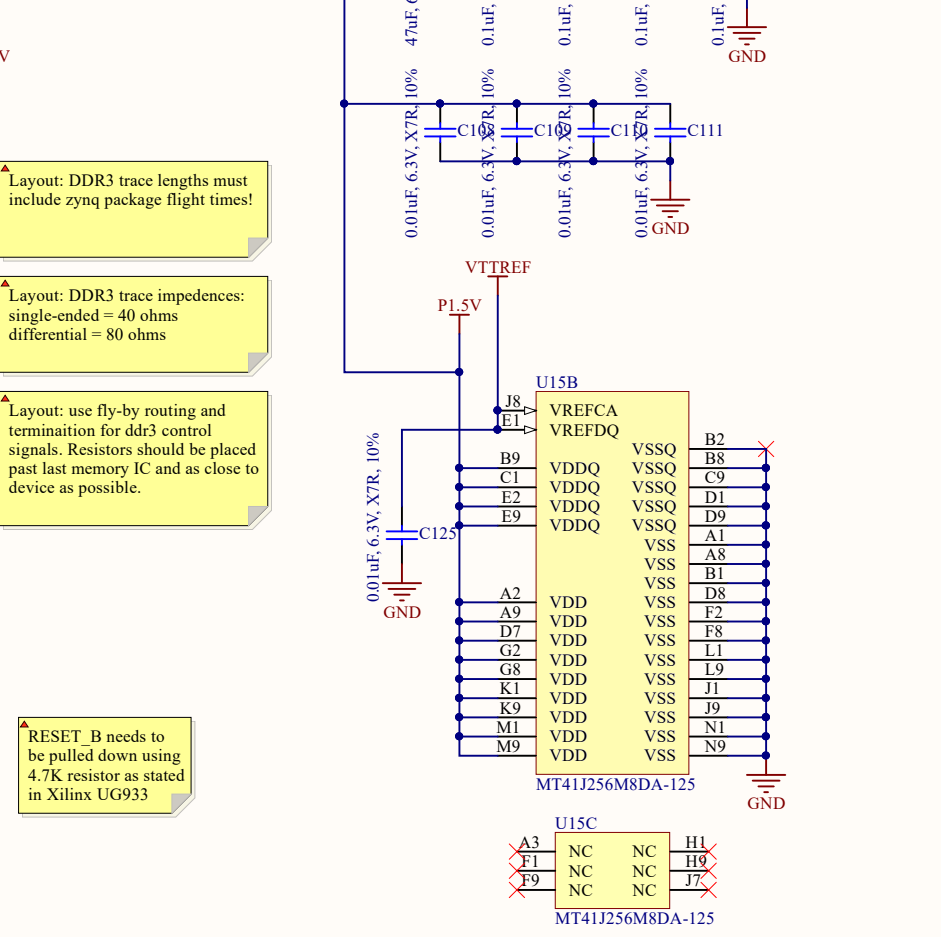
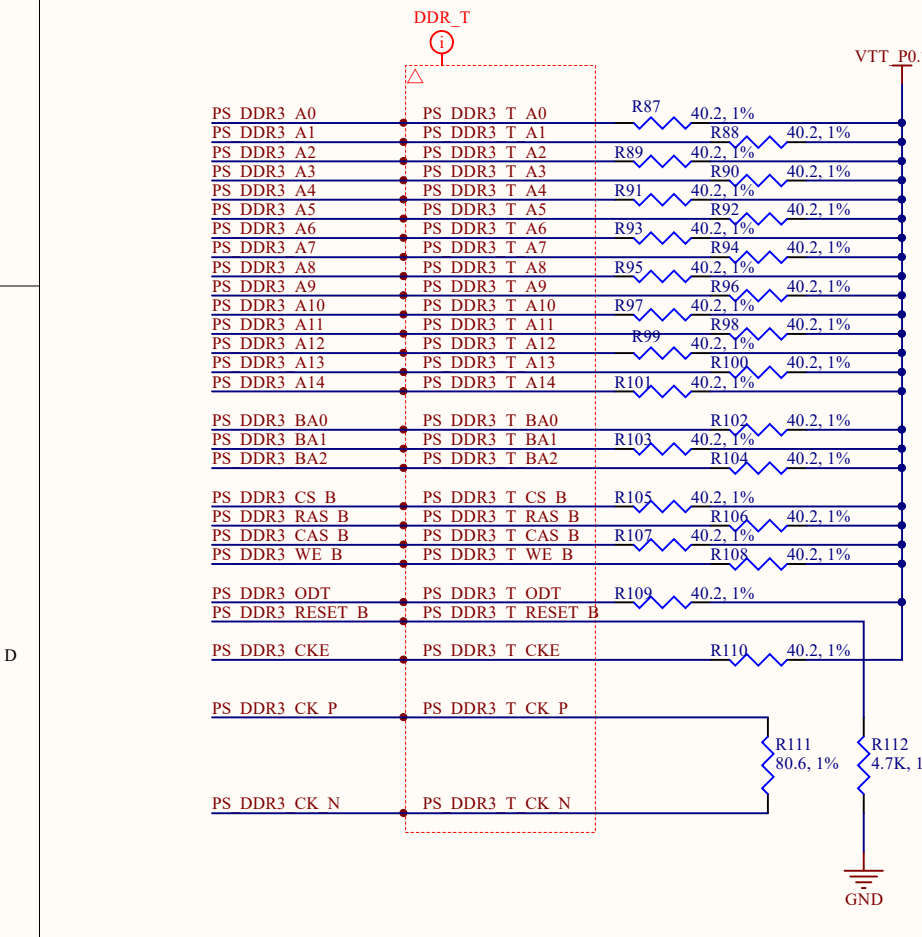
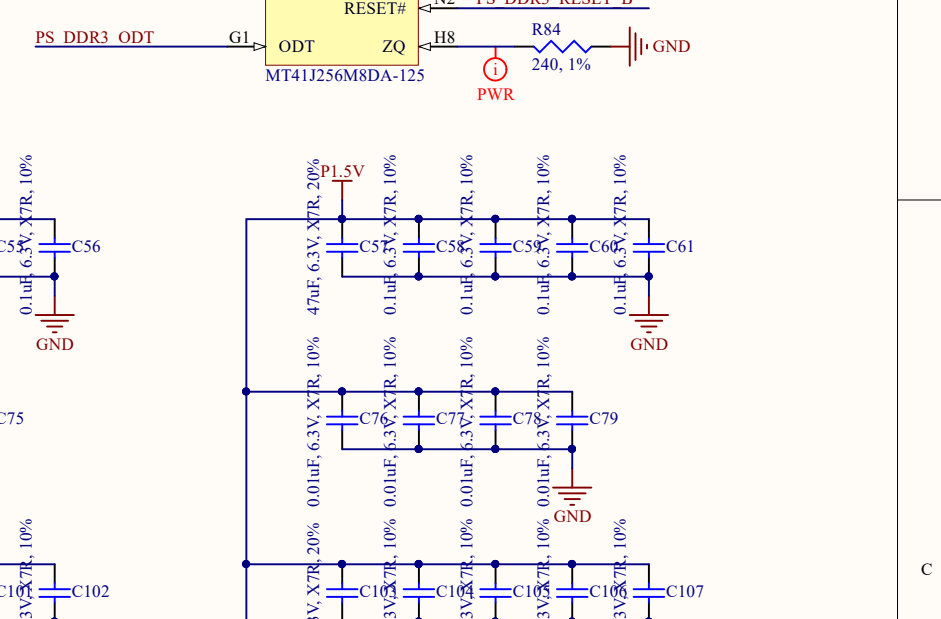
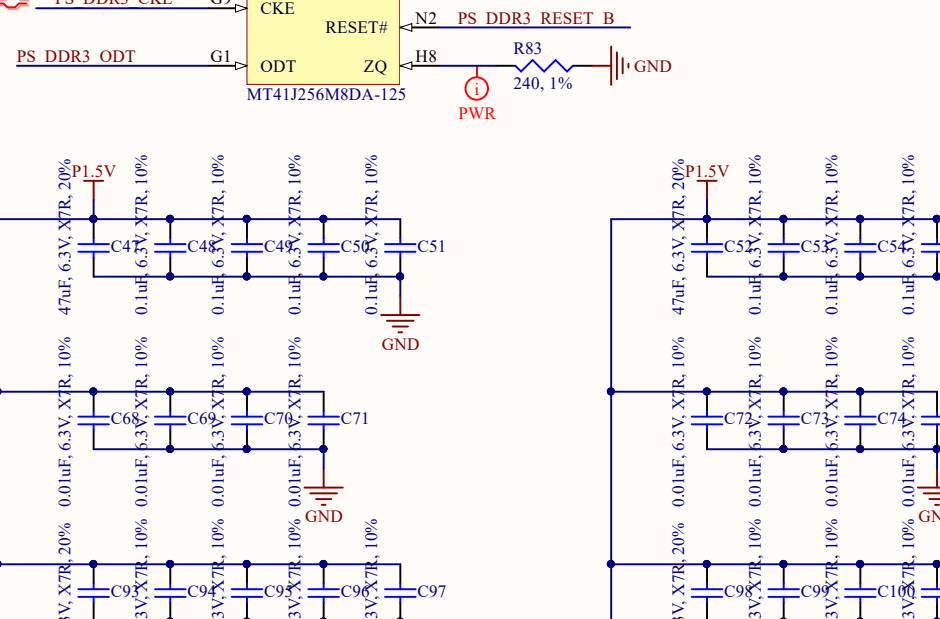
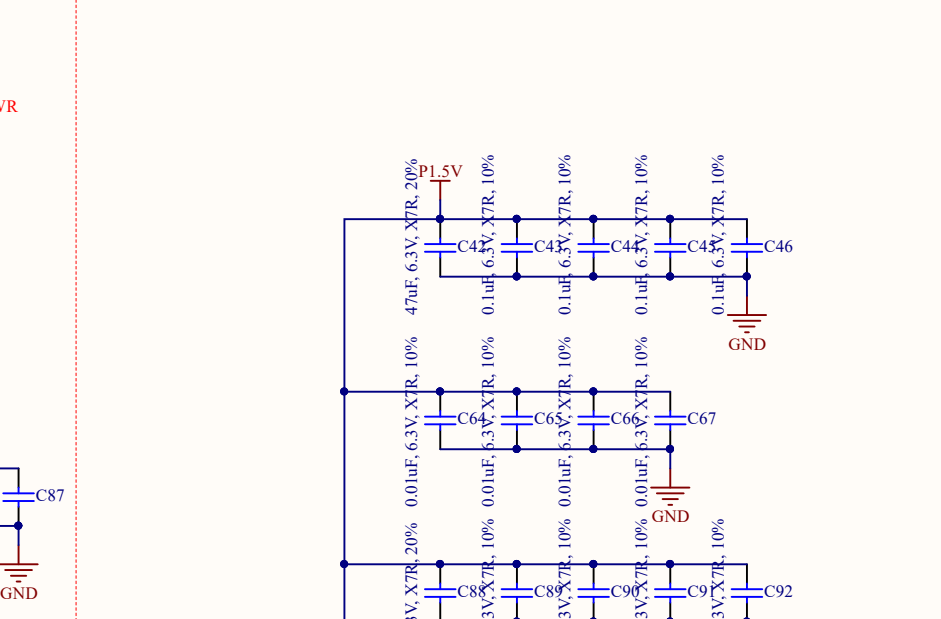
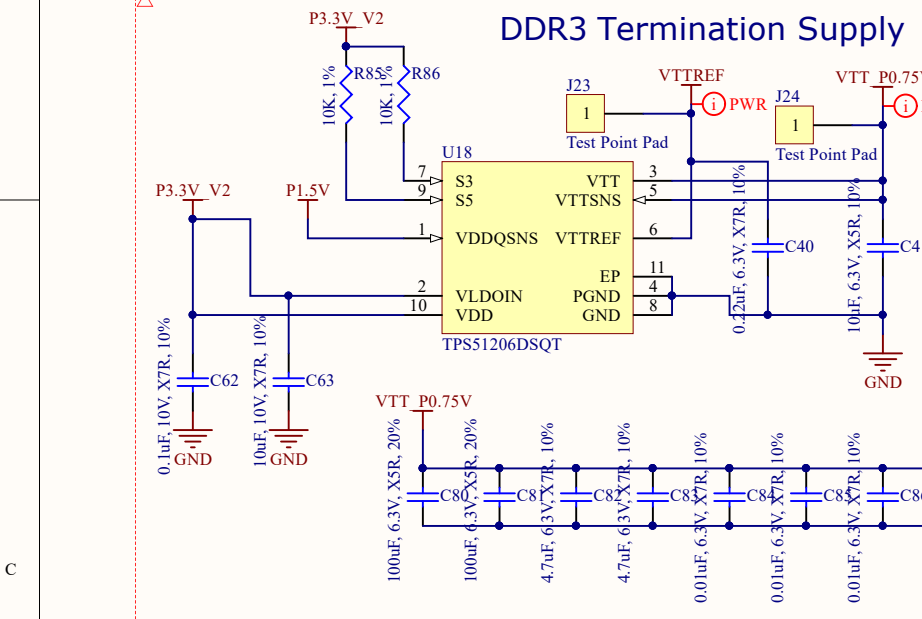
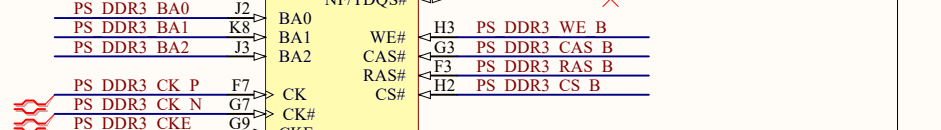
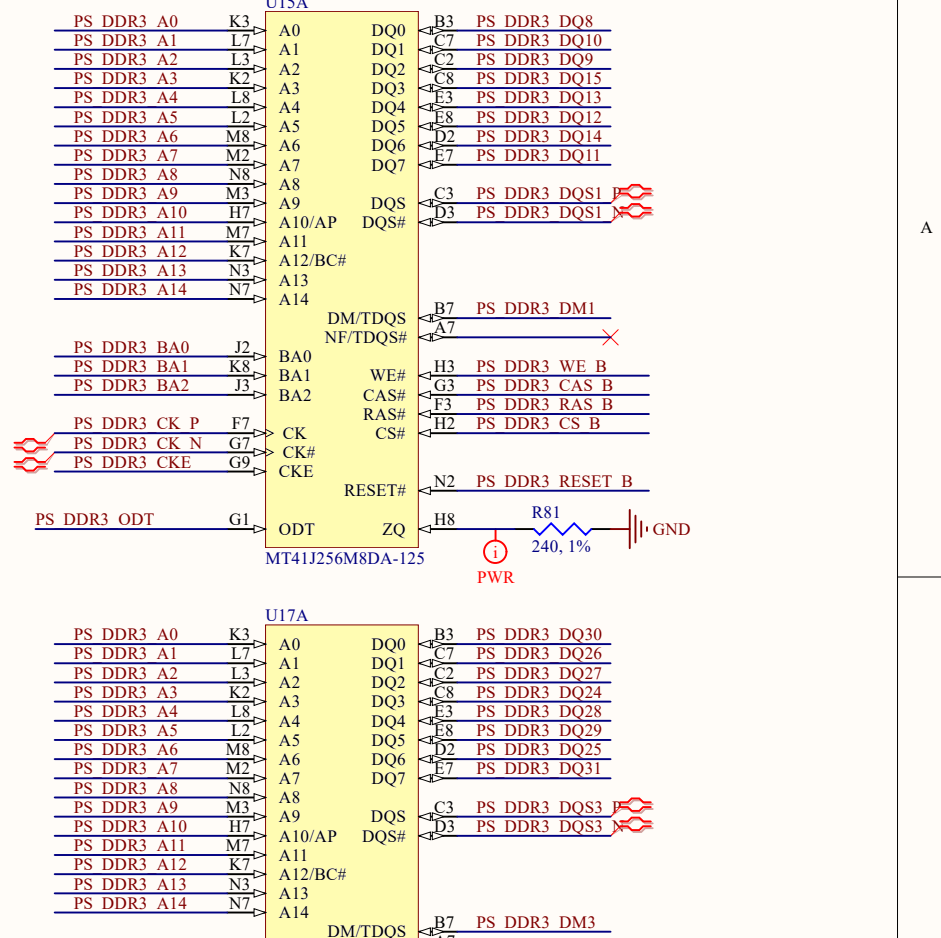
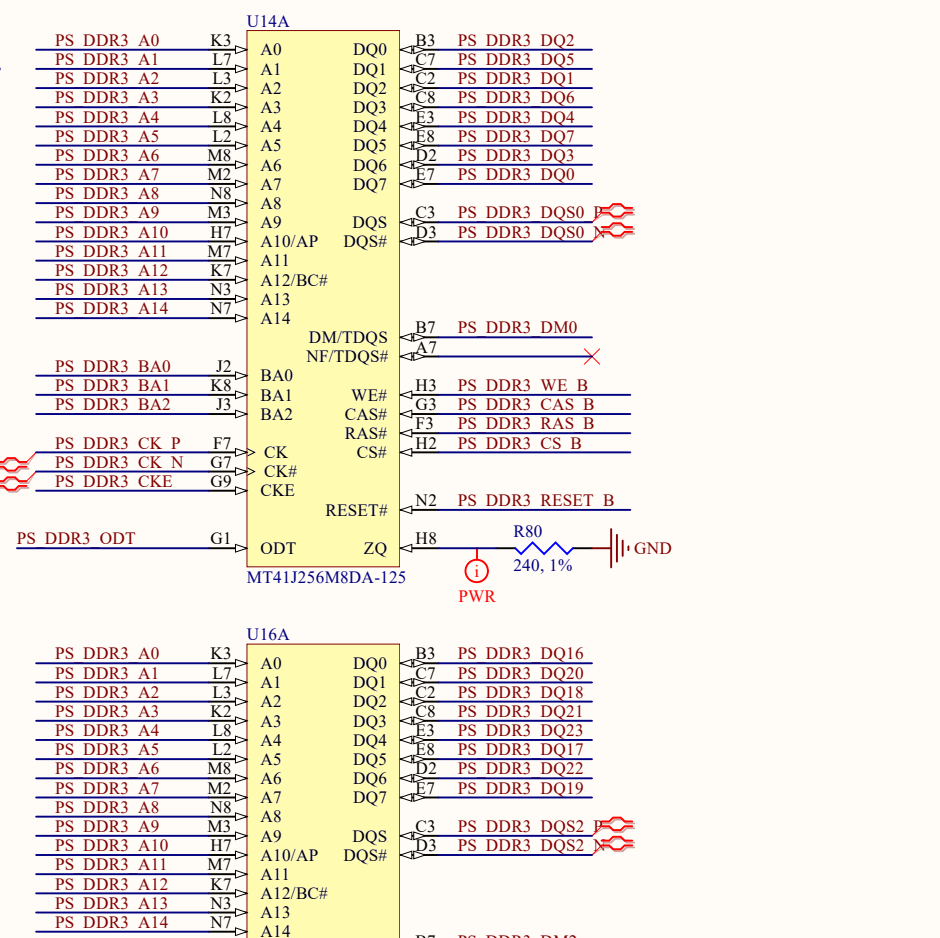
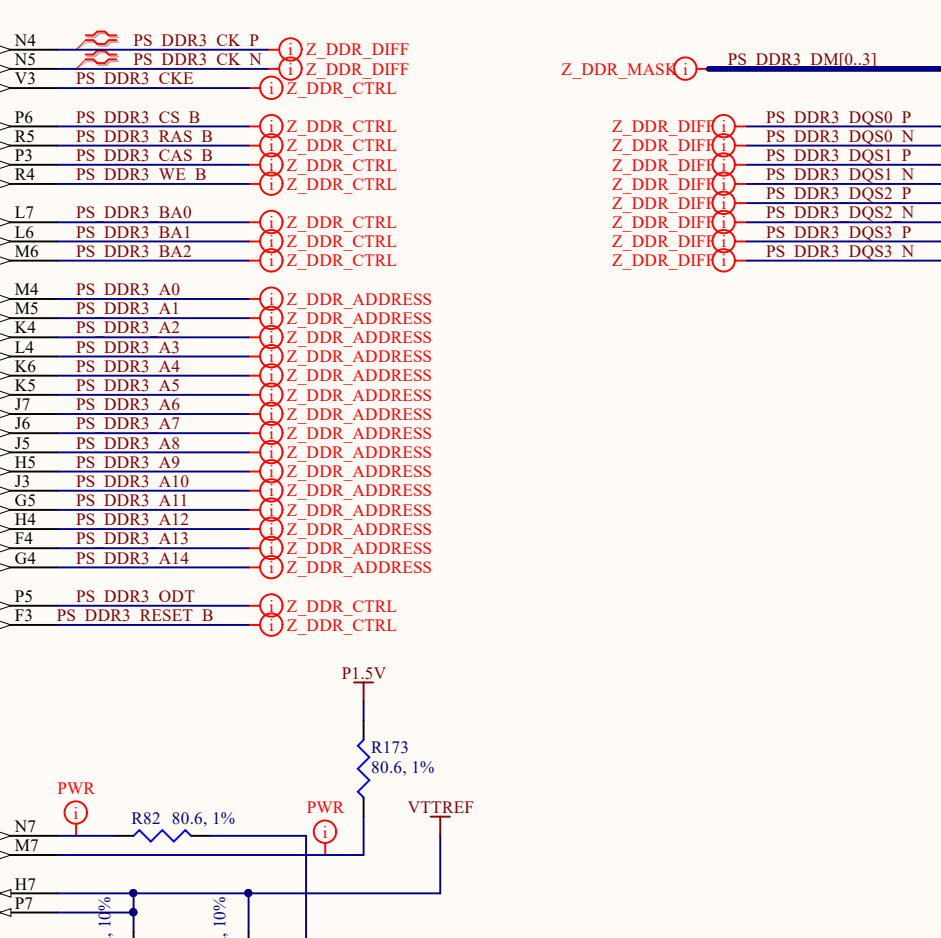
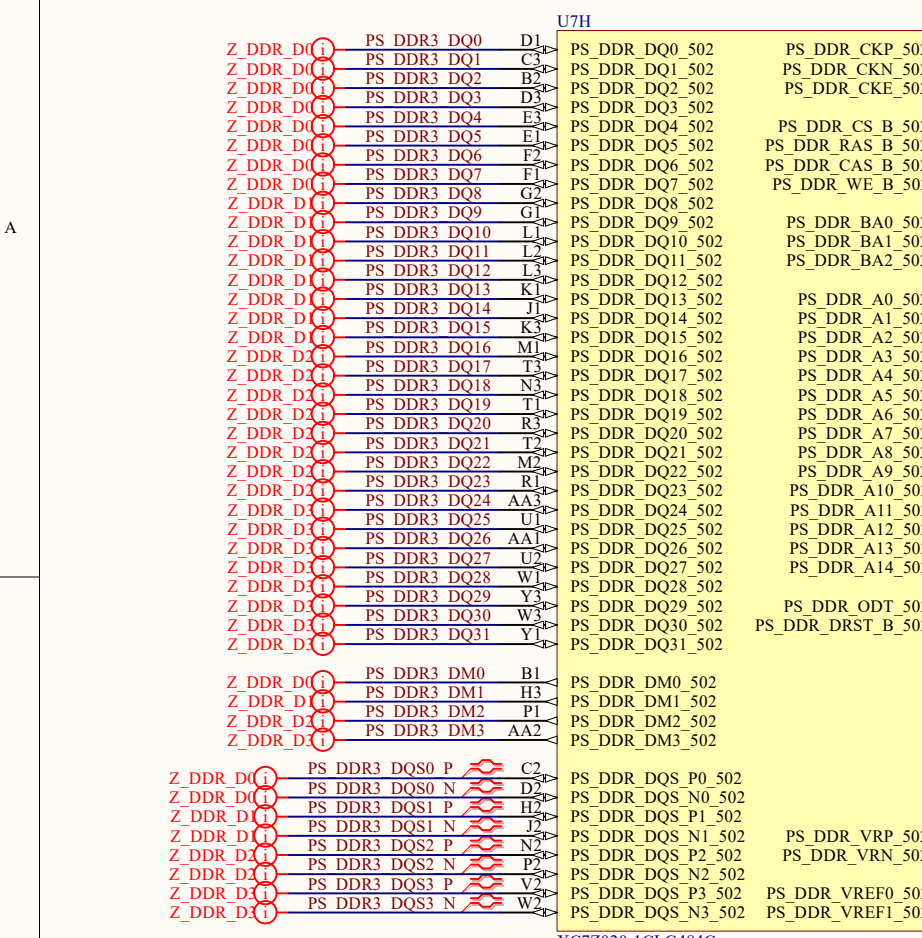
XC7Z020-1CLG484C

High-Speed Expansion Port



7-Series devices with only HR banks (no HP), only support LVDS25 for bidirectional use. This includes the zynq and also the artix devices.



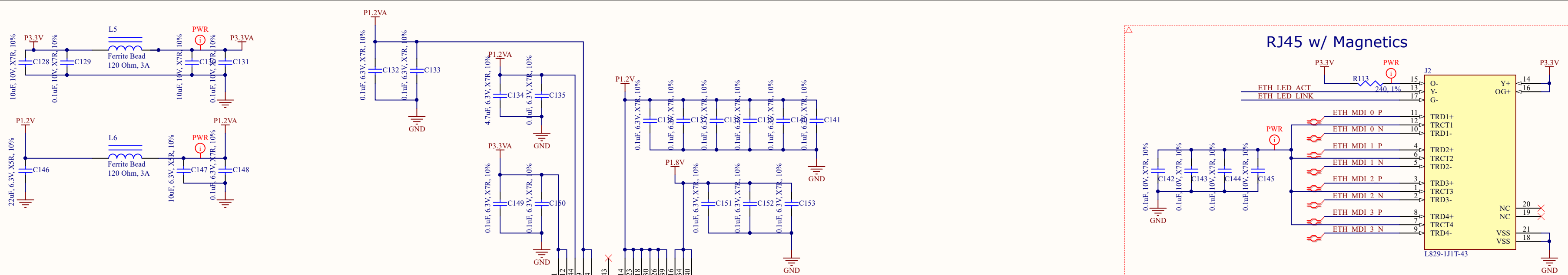


Layout: DDR3 trace lengths must include zynq package flight times!

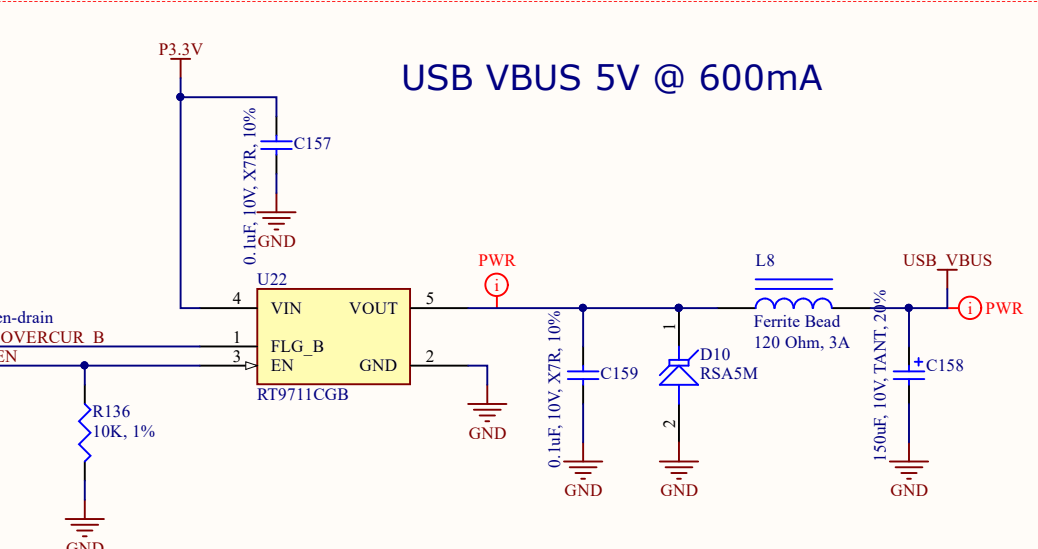
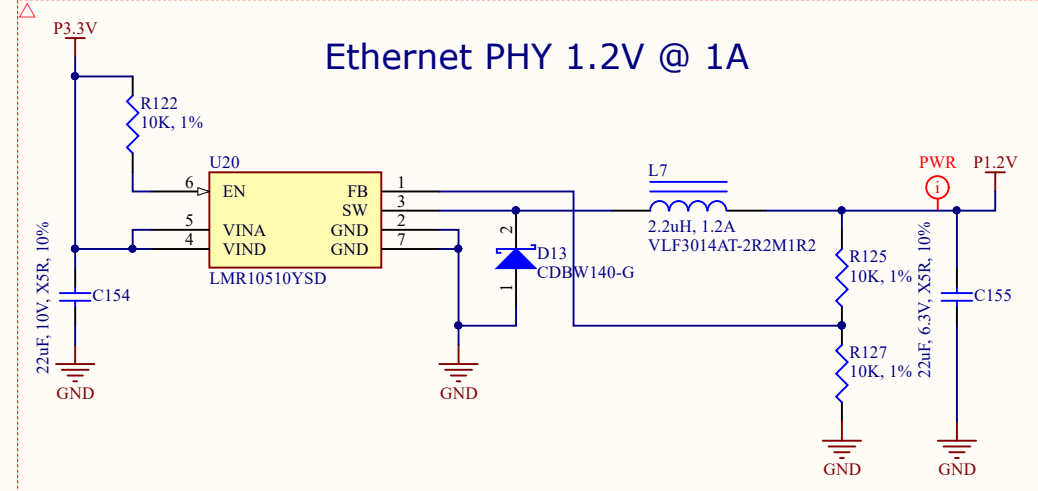
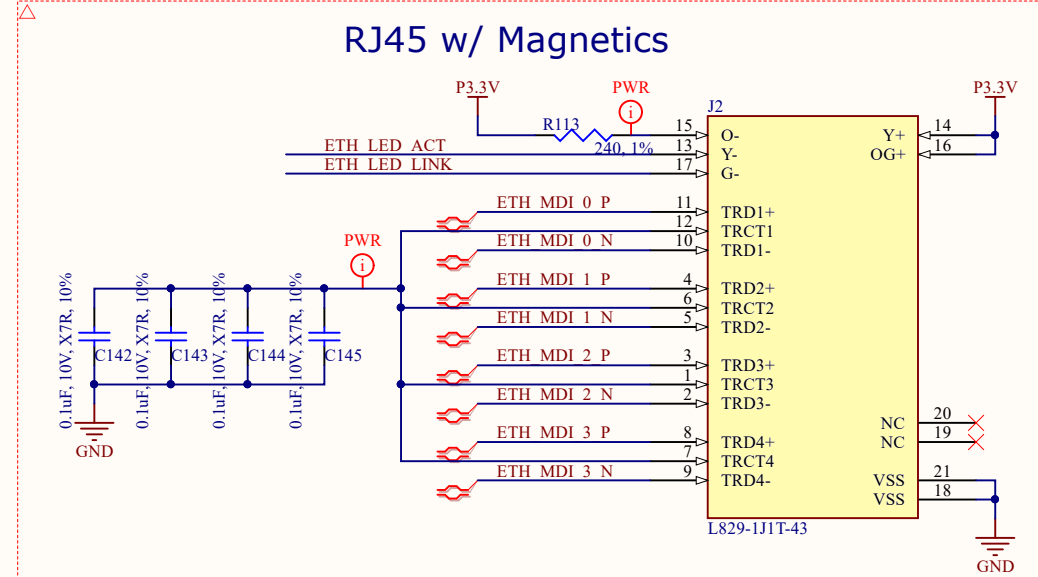
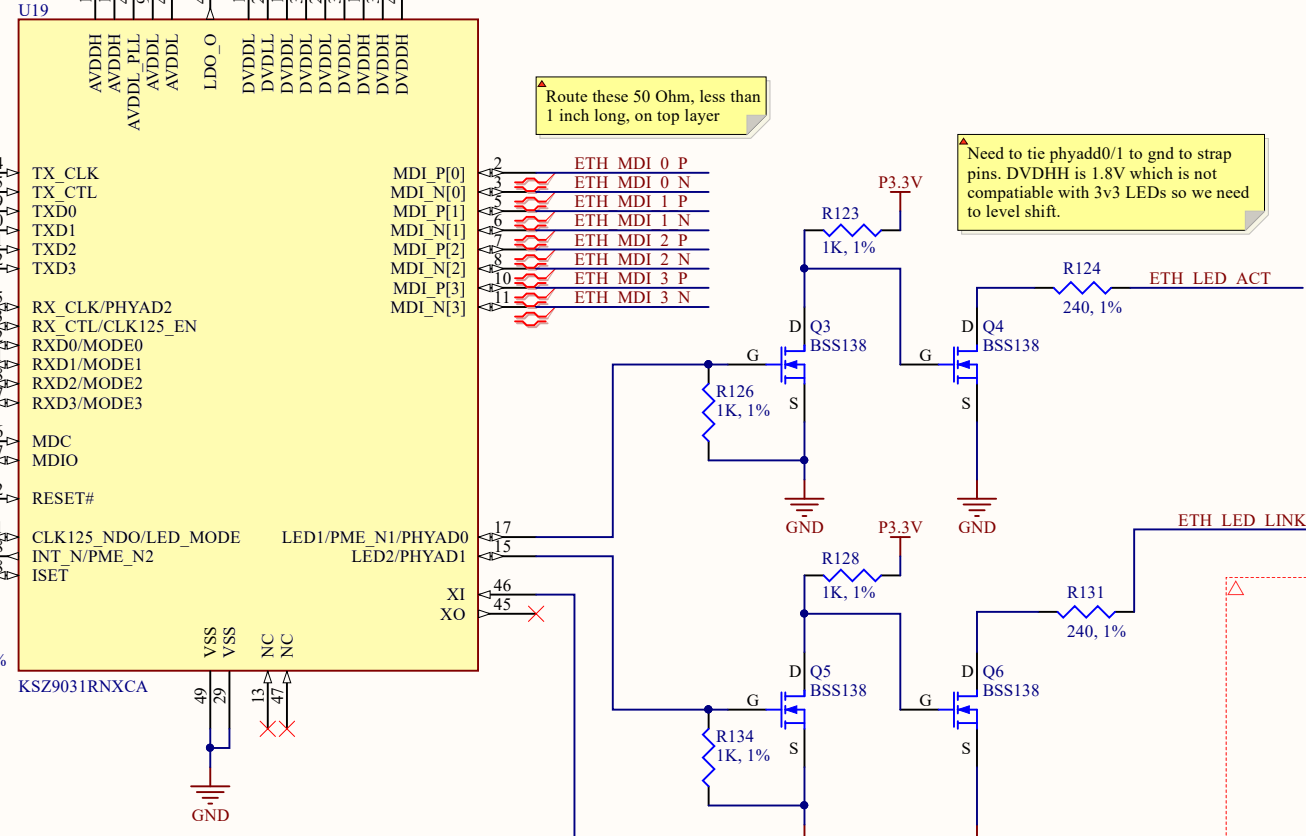
Layout: DDR3 trace impedances: single-ended = 40 ohms differential = 80 ohms

Layout: use fly-by routing and termination for ddr3 control signals. Resistors should be placed past last memory IC and as close to device as possible.

RESET_B needs to be pulled down using 4.7K resistor as stated in Xilinx UG6933



Gigabit Ethernet PHY



phy strap pins
 PHYAD1 - 15 - low
 PHYAD0 - 17 - low
 PHYAD2 - 35 - low
 MODE3 - 27 - high
 MODE2 - 28 - high
 MODE1 - 31 - high
 MODE0 - 32 - high
 CLK125_EN - 33 - low
 LED_MODE - 41 - high

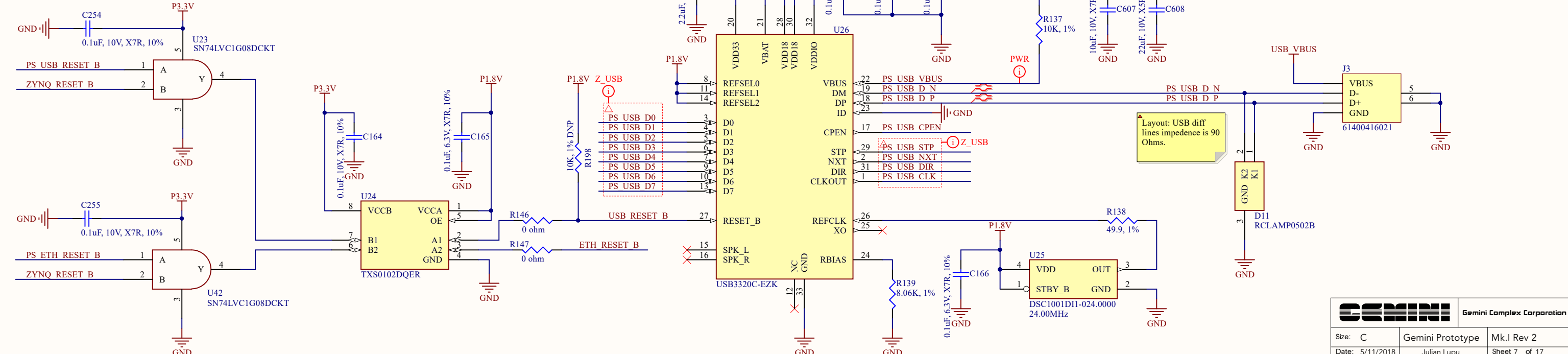
phy address 0b0000
 mode 1111 - RGMII advertise all capabilities
 clk125 - disable
 led mode - single-led mode

ZYNQ_POR_B is connected to the power good of the last 3.3v rail that goes high and will remain high after. The usb and ethernet controller's reset is ANDed with the ZYNQ_POR_B so it will only accept resets when power is good.

ZYNQ_RESET_B is an AND of ZYNQ_POR_B and ZYNQ_SRST_B_P3.3V

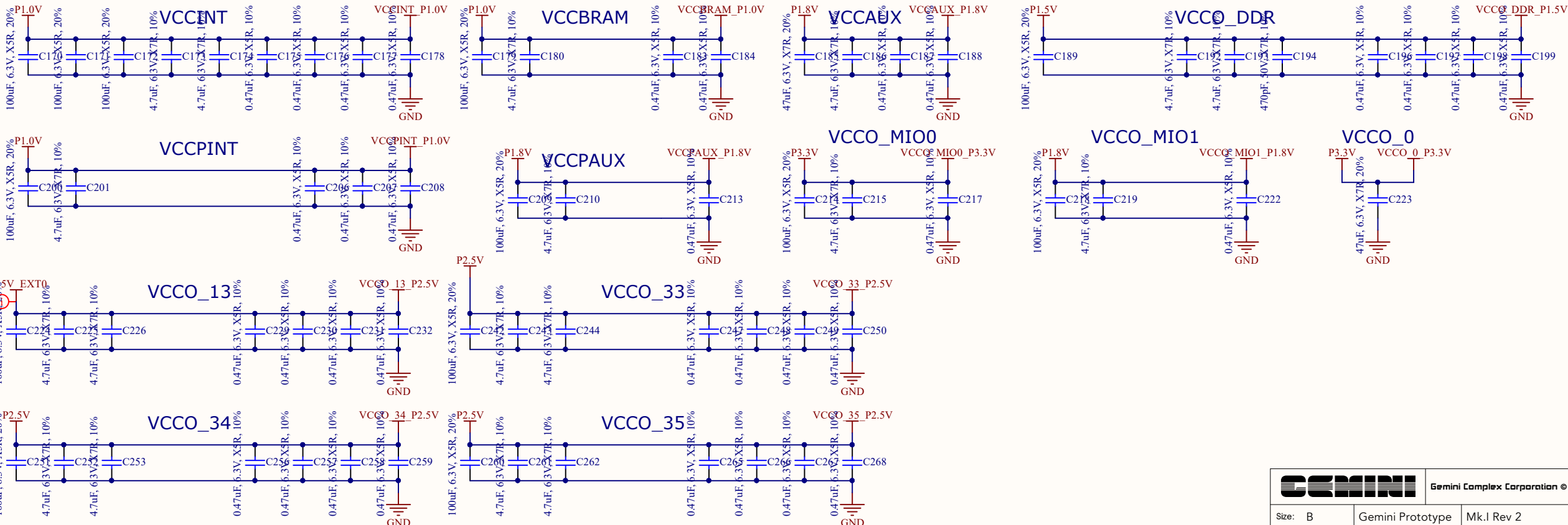
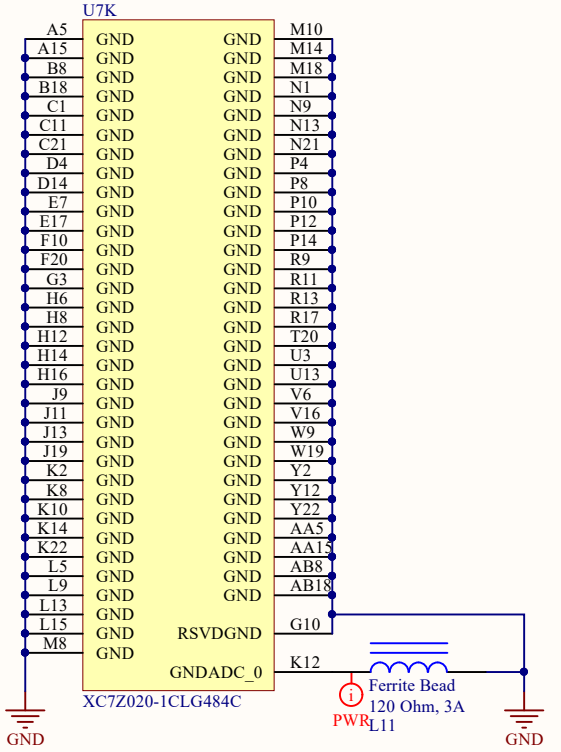
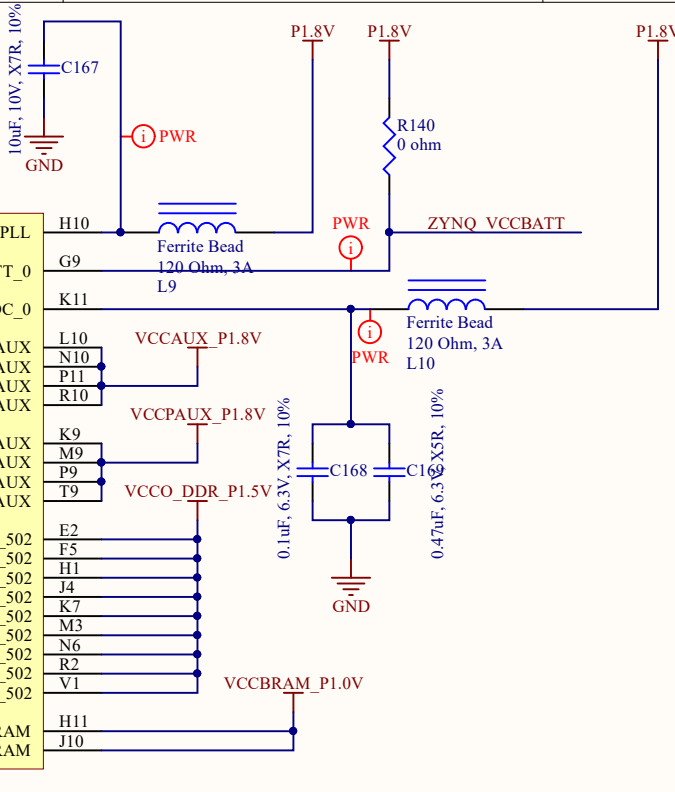
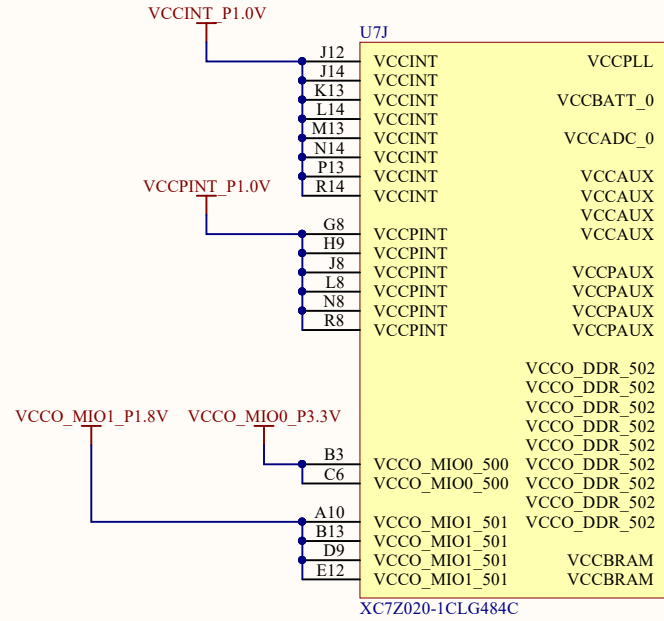
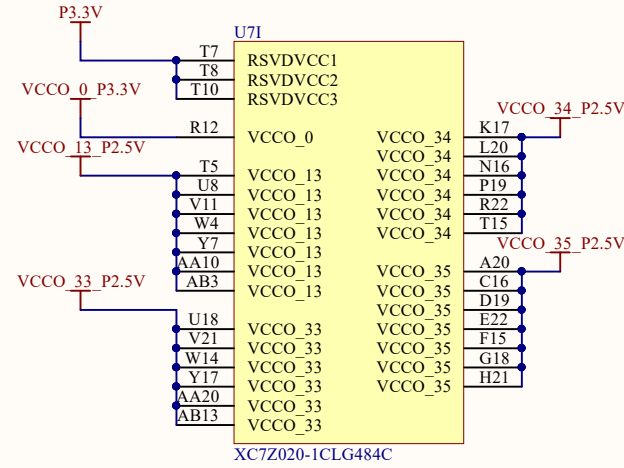
PS_USB_RESET_B operates at 3.3v so it's good.
 PS_ETH_RESET_B operates at 3.3v so it's good.
 ZYNQ_RESET_B will reset both usb and eth.

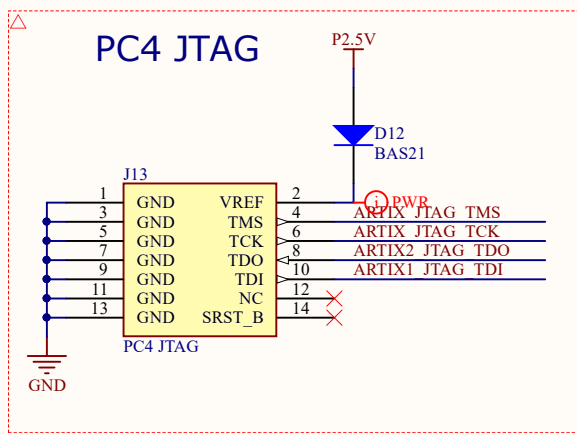
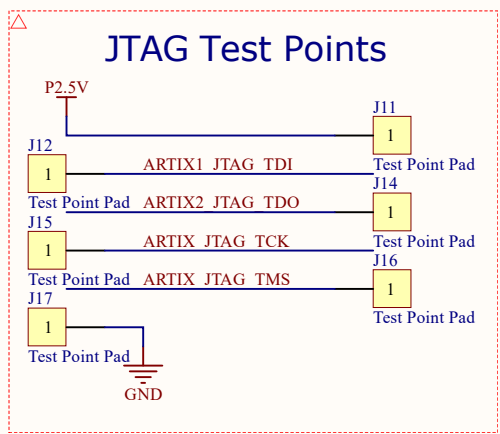
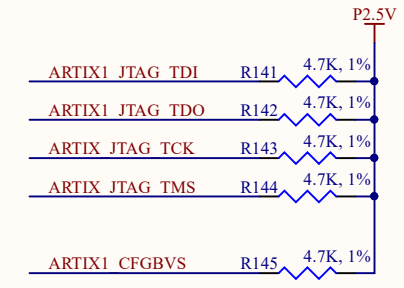
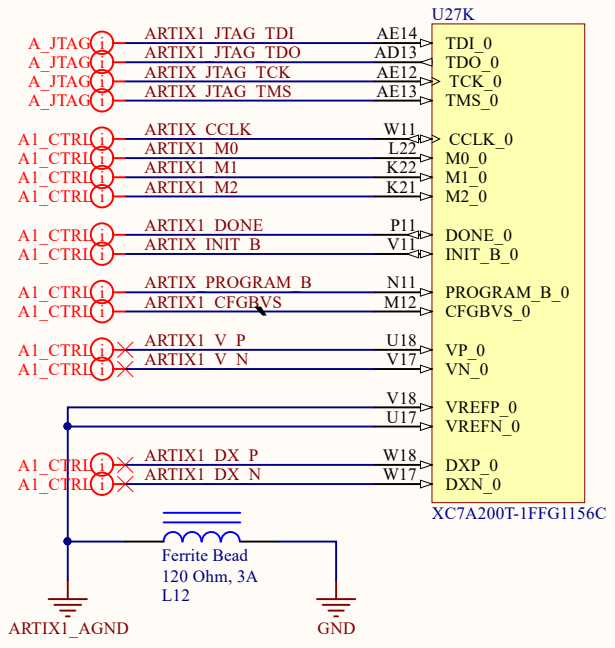
USB 2.0 PHY - Host Mode



Banks 13 have their voltage supplies set by the interposer card depending on what it's being connected to.

Banks 33, 34 and 35 are connected to the artix units, which operate at 2.5v.



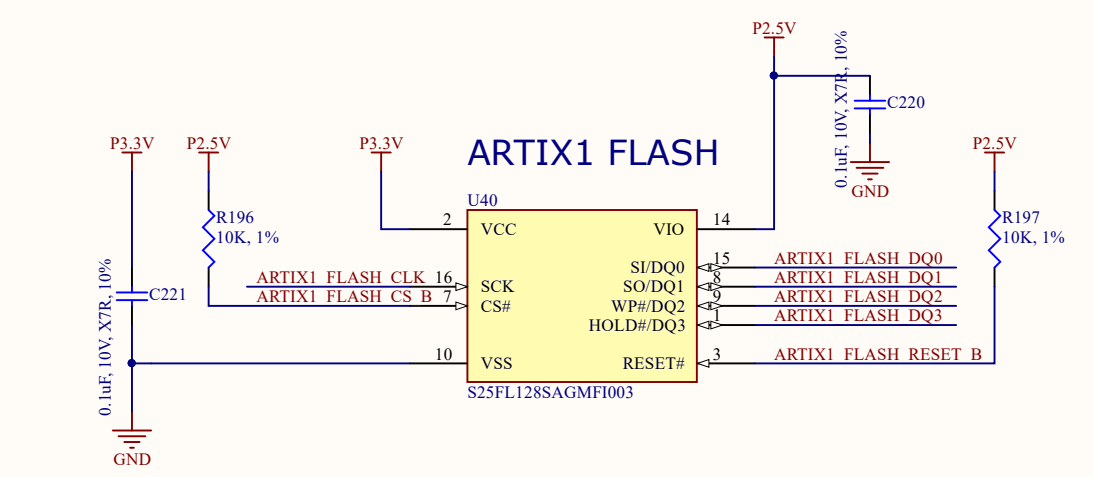
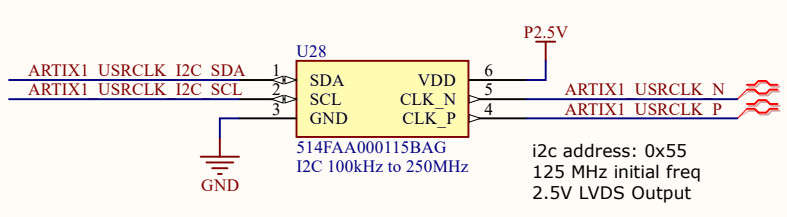
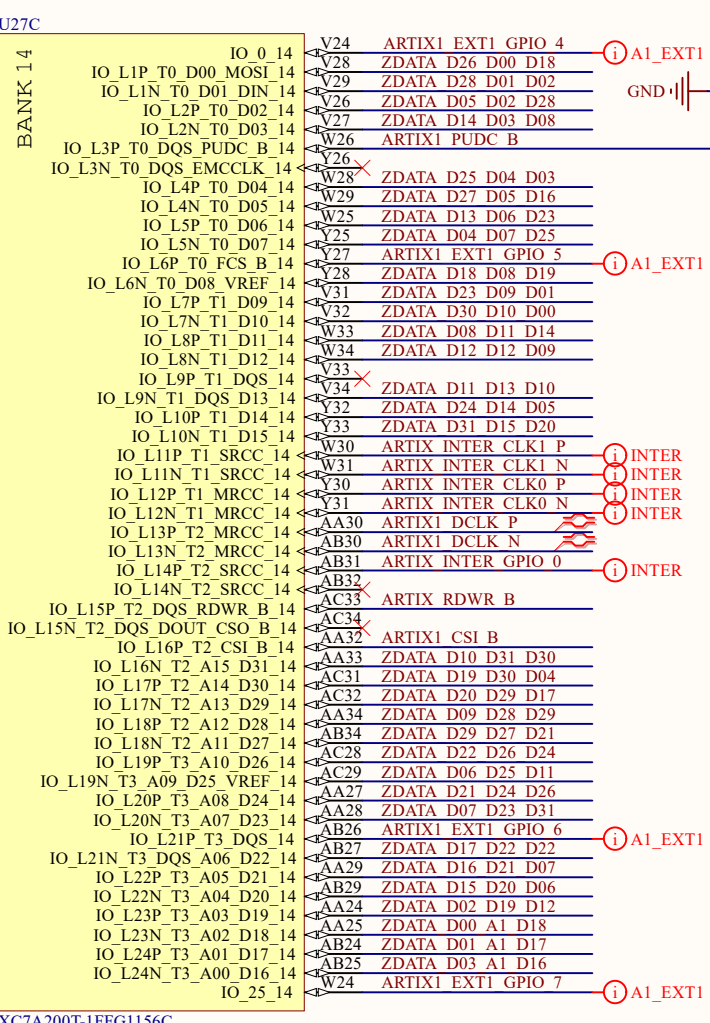
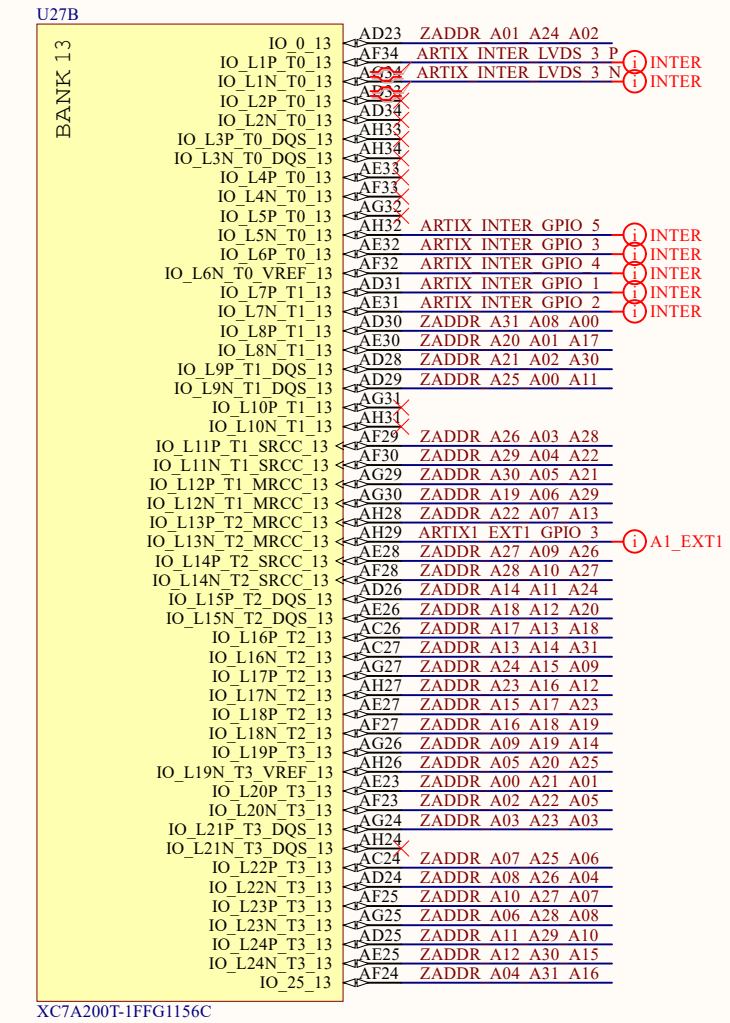
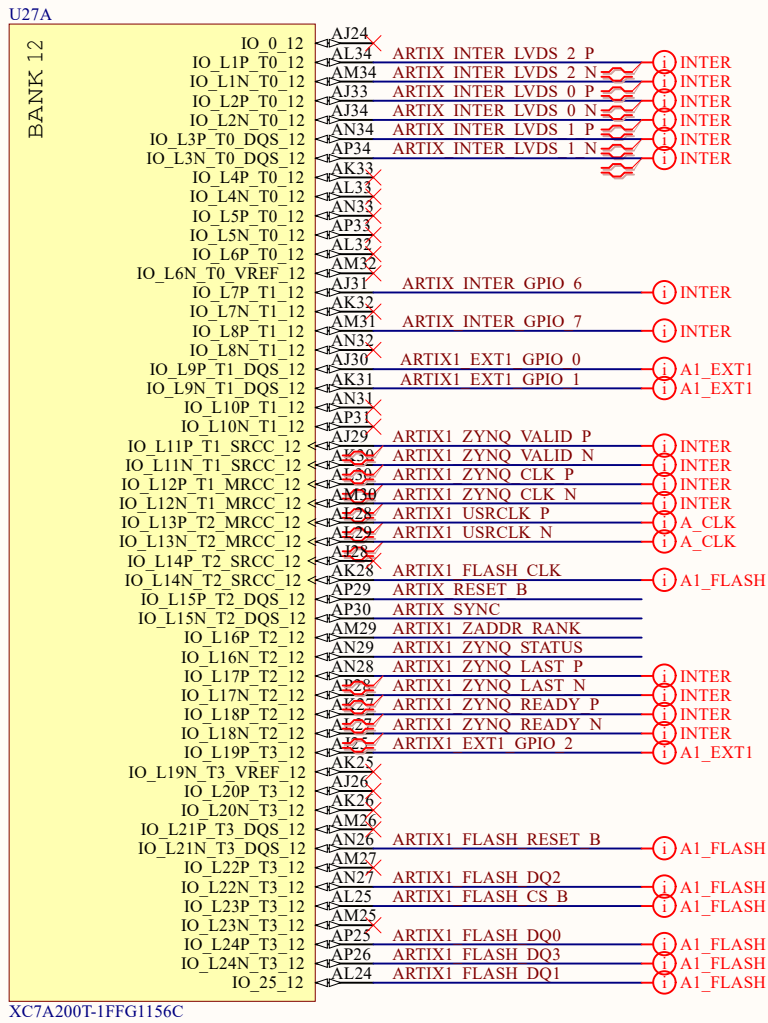
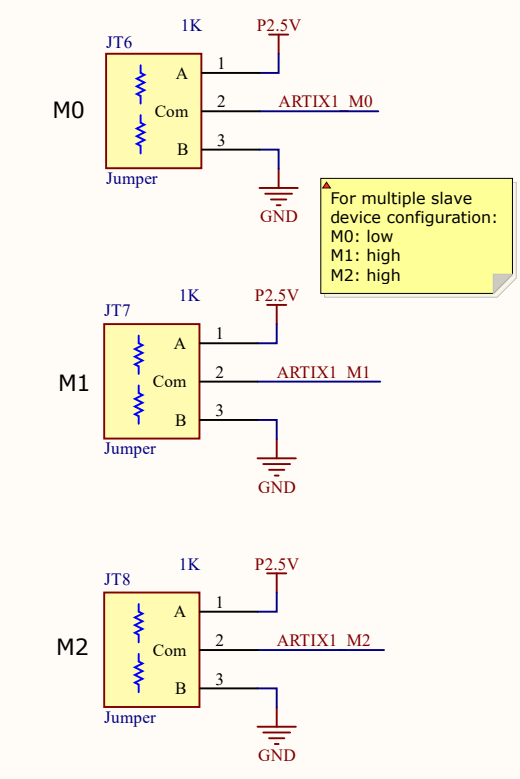


JTAG is daisy-chained from artix1 to artix2.

PC4 TDI -> ARTIX1_TDI -> ARTIX1_TDO -> ARTIX2_TDI -> ARTIX2_TDO -> PC4_TDO

Default: Pull-high: pin 1-2 with a 1k Ohm.

Pulling PUDC_B high will float the IO pins during configuration.



A

A

A1_DUT_IO

BANK 35		U271	R11	ARTIX1 DUT IO 51
		M7	ARTIX1 DUT IO 78	
IO_0_35	M6	ARTIX1 DUT IO 65		
IO_L1P_T0_AD4P_35	N9	ARTIX1 DUT IO 48		
IO_L1N_T0_AD4N_35	M9	ARTIX1 DUT IO 50		
IO_L2P_T0_AD12P_35	N8	ARTIX1 DUT IO 58		
IO_L2N_T0_AD12N_35	M8	ARTIX1 DUT IO 66		
IO_L3P_T0_DQS_AD5P_35	N7	ARTIX1 DUT IO 61		
IO_L3N_T0_DQS_AD5N_35	M11	ARTIX1 DUT IO 60		
IO_L4P_T0_35	M10	ARTIX1 DUT IO 60		
IO_L4N_T0_35	N9	ARTIX1 DUT IO 59		
IO_L5P_T0_AD13P_35	P8	ARTIX1 DUT IO 68		
IO_L5N_T0_AD13N_35	P6	ARTIX1 DUT IO 76		
IO_L6P_T0_35	N6	ARTIX1 DUT IO 55		
IO_L6N_T0_VREF_35	N1	ARTIX1 DUT IO 33		
IO_L7P_T1_AD6P_35	M1	ARTIX1 DUT IO 90		
IO_L7N_T1_AD6N_35	M5	ARTIX1 DUT IO 28		
IO_L8P_T1_AD14P_35	M4	ARTIX1 DUT IO 6		
IO_L8N_T1_AD14N_35	R1	ARTIX1 DUT IO 32		
IO_L9P_T1_DQS_AD7P_35	P1	ARTIX1 DUT IO 31		
IO_L9N_T1_DQS_AD7N_35	N3	ARTIX1 DUT IO 26		
IO_L10P_T1_AD15P_35	N2	ARTIX1 DUT IO 4		
IO_L10N_T1_AD15N_35	P4	ARTIX1 DUT IO 13		
IO_L11P_T1_SRCC_35	P3	ARTIX1 DUT IO 3		
IO_L11N_T1_SRCC_35	P5	ARTIX1 DUT IO 35		
IO_L12P_T1_MRCC_35	N4	ARTIX1 DUT IO 5		
IO_L12N_T1_MRCC_35	R6	ARTIX1 DUT IO 64		
IO_L13P_T2_MRCC_35	R5	ARTIX1 DUT IO 24		
IO_L13N_T2_MRCC_35	R5	ARTIX1 DUT IO 2		
IO_L14P_T2_SRCC_35	T4	ARTIX1 DUT IO 1		
IO_L14N_T2_SRCC_35	R3	ARTIX1 DUT IO 12		
IO_L15P_T2_DQS_35	R2	ARTIX1 DUT IO 23		
IO_L15N_T2_DQS_35	U2	ARTIX1 DUT IO 30		
IO_L16P_T2_35	U1	ARTIX1 DUT IO 20		
IO_L16N_T2_35	T3	ARTIX1 DUT IO 11		
IO_L17P_T2_35	T2	ARTIX1 DUT IO 21		
IO_L17N_T2_35	U5	ARTIX1 DUT IO 10		
IO_L18P_T2_35	U4	ARTIX1 DUT IO 22		
IO_L18N_T2_35	R8	ARTIX1 DUT IO 67		
IO_L19P_T3_35	R7	ARTIX1 DUT IO 56		
IO_L19N_T3_VREF_35	R10	ARTIX1 DUT IO 52		
IO_L20P_T3_35	P10	ARTIX1 DUT IO 72		
IO_L20N_T3_35	U10	ARTIX1 DUT IO 74		
IO_L21P_T3_DQS_35	T10	ARTIX1 DUT IO 62		
IO_L21N_T3_DQS_35	U7	ARTIX1 DUT IO 63		
IO_L22P_T3_35	U6	ARTIX1 DUT IO 0		
IO_L22N_T3_35	T8	ARTIX1 DUT IO 57		
IO_L23P_T3_35	T7	ARTIX1 DUT IO 54		
IO_L23N_T3_35	U9	ARTIX1 DUT IO 128		
IO_L24P_T3_35	T9	ARTIX1 DUT IO 69		
IO_L24N_T3_35	U11	ARTIX1 DUT IO 53		
IO_25_35				

XC7A200T-1FFG1156C

A1_DUT_IO

BANK 36		U27J	H12	ARTIX1 DUT IO 88
		K12	ARTIX1 DUT IO 89	
IO_0_36	G10	ARTIX1 DUT IO 43		
IO_L1P_T0_36	G9	ARTIX1 DUT IO 42		
IO_L1N_T0_36	K11	ARTIX1 DUT IO 46		
IO_L2P_T0_36	H11	ARTIX1 DUT IO 45		
IO_L2N_T0_36	G11	ARTIX1 DUT IO 77		
IO_L3P_T0_DQS_36	L10	ARTIX1 DUT IO 79		
IO_L3N_T0_DQS_36	L9	ARTIX1 DUT IO 85		
IO_L4P_T0_36	K10	ARTIX1 DUT IO 44		
IO_L4N_T0_36	J10	ARTIX1 DUT IO 86		
IO_L5P_T0_36	J9	ARTIX1 DUT IO 84		
IO_L5N_T0_36	H8	ARTIX1 DUT IO 83		
IO_L6P_T0_36	H9	ARTIX1 DUT IO 75		
IO_L6N_T0_VREF_36	H8	ARTIX1 DUT IO 41		
IO_L7P_T1_36	L8	ARTIX1 DUT IO 19		
IO_L7N_T1_36	K8	ARTIX1 DUT IO 9		
IO_L8P_T1_36	G7	ARTIX1 DUT IO 40		
IO_L8N_T1_36	G6	ARTIX1 DUT IO 99		
IO_L9P_T1_DQS_36	K7	ARTIX1 DUT IO 70		
IO_L9N_T1_DQS_36	K6	ARTIX1 DUT IO 8		
IO_L10P_T1_36	H7	ARTIX1 DUT IO 73		
IO_L10N_T1_36	H6	ARTIX1 DUT IO 82		
IO_L11P_T1_SRCC_36	G5	ARTIX1 DUT IO 71		
IO_L11N_T1_SRCC_36	G4	ARTIX1 DUT IO 97		
IO_L12P_T1_MRCC_36	J6	ARTIX1 DUT IO 81		
IO_L12N_T1_MRCC_36	J5	ARTIX1 DUT IO 98		
IO_L13P_T2_MRCC_36	T3	ARTIX1 DUT IO 96		
IO_L13N_T2_MRCC_36	F2	ARTIX1 DUT IO 37		
IO_L14P_T2_SRCC_36	L5	ARTIX1 DUT IO 17		
IO_L14N_T2_SRCC_36	K5	ARTIX1 DUT IO 7		
IO_L15P_T2_DQS_36	H4	ARTIX1 DUT IO 80		
IO_L15N_T2_DQS_36	H3	ARTIX1 DUT IO 29		
IO_L16P_T2_36	J4	ARTIX1 DUT IO 39		
IO_L16N_T2_36	J3	ARTIX1 DUT IO 38		
IO_L17P_T2_36	L4	ARTIX1 DUT IO 16		
IO_L17N_T2_36	L3	ARTIX1 DUT IO 15		
IO_L18P_T2_36	H2	ARTIX1 DUT IO 95		
IO_L18N_T2_36	G2	ARTIX1 DUT IO 27		
IO_L19P_T3_36	K1	ARTIX1 DUT IO 92		
IO_L19N_T3_VREF_36	J1	ARTIX1 DUT IO 91		
IO_L20P_T3_36	H1	ARTIX1 DUT IO 36		
IO_L20N_T3_36	G1	ARTIX1 DUT IO 25		
IO_L21P_T3_DQS_36	M2	ARTIX1 DUT IO 14		
IO_L21N_T3_DQS_36	L2	ARTIX1 DUT IO 34		
IO_L22P_T3_36	K3	ARTIX1 DUT IO 94		
IO_L22N_T3_36	K2	ARTIX1 DUT IO 93		
IO_L23P_T3_36	L7	ARTIX1 DUT IO 18		
IO_L23N_T3_36				
IO_L24P_T3_36				
IO_L24N_T3_36				
IO_25_36				

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A1_DUT_IO

BANK 15		U27D	T24	ARTIX1 DUT IO 133
		P26	ARTIX1 DUT IO 148	
IO_0_15	N26	ARTIX1 DUT IO 149		
IO_L1P_T0_AD0P_15	M27	ARTIX1 DUT IO 123		
IO_L1N_T0_AD0N_15	U25	ARTIX1 DUT IO 144		
IO_L2P_T0_AD8P_15	T25	ARTIX1 DUT IO 145		
IO_L2N_T0_AD8N_15	P24	ARTIX1 DUT IO 135		
IO_L3P_T0_DQS_AD1P_15	N24	ARTIX1 DUT IO 137		
IO_L3N_T0_DQS_AD1N_15	U26	ARTIX1 DUT IO 141		
IO_L4P_T0_15	U25	ARTIX1 DUT IO 193		
IO_L4N_T0_15	R25	ARTIX1 DUT IO 139		
IO_L5P_T0_AD9P_15	P25	ARTIX1 DUT IO 136		
IO_L5N_T0_AD9N_15	T27	ARTIX1 DUT IO 179		
IO_L6P_T0_15	R27	ARTIX1 DUT IO 192		
IO_L6N_T0_VREF_15	N27	ARTIX1 DUT IO 138		
IO_L7P_T1_AD2P_15	N28	ARTIX1 DUT IO 124		
IO_L7N_T1_AD2N_15	U28	ARTIX1 DUT IO 183		
IO_L8P_T1_AD10P_15	R28	ARTIX1 DUT IO 181		
IO_L8N_T1_AD10N_15	N29	ARTIX1 DUT IO 164		
IO_L9P_T1_DQS_AD3P_15	M29	ARTIX1 DUT IO 126		
IO_L9N_T1_DQS_AD3N_15	U29	ARTIX1 DUT IO 194		
IO_L10P_T1_AD11P_15	T29	ARTIX1 DUT IO 195		
IO_L10N_T1_AD11N_15	P28	ARTIX1 DUT IO 165		
IO_L11P_T1_SRCC_15	N29	ARTIX1 DUT IO 182		
IO_L11N_T1_SRCC_15	R30	ARTIX1 DUT IO 187		
IO_L12P_T1_MRCC_15	P30	ARTIX1 DUT IO 166		
IO_L12N_T1_MRCC_15	U30	ARTIX1 DUT IO 185		
IO_L13P_T2_MRCC_15	T30	ARTIX1 DUT IO 196		
IO_L13N_T2_MRCC_15	M30	ARTIX1 DUT IO 178		
IO_L14P_T2_SRCC_15	R31	ARTIX1 DUT IO 157		
IO_L14N_T2_SRCC_15	P31	ARTIX1 DUT IO 197		
IO_L15P_T2_DQS_15	N31	ARTIX1 DUT IO 167		
IO_L15N_T2_DQS_ADV_B_15	M32	ARTIX1 DUT IO 158		
IO_L16P_T2_A28_15	U31	ARTIX1 DUT IO 189		
IO_L16N_T2_A27_15	U32	ARTIX1 DUT IO 199		
IO_L17P_T2_A26_15	T32	ARTIX1 DUT IO 198		
IO_L17N_T2_A25_15	R32	ARTIX1 DUT IO 191		
IO_L18P_T2_A24_15	N32	ARTIX1 DUT IO 161		
IO_L18N_T2_A23_15	U33	ARTIX1 DUT IO 184		
IO_L19P_T3_A22_15	T33	ARTIX1 DUT IO 190		
IO_L19N_T3_A21_VREF_15	R33	ARTIX1 DUT IO 175		
IO_L20P_T3_A20_15	N34	ARTIX1 DUT IO 168		
IO_L20N_T3_A19_15	M34	ARTIX1 DUT IO 172		
IO_L21P_T3_DQS_15	U34	ARTIX1 DUT IO 176		
IO_L21N_T3_DQS_A18_15	T34	ARTIX1 DUT IO 177		
IO_L22P_T3_A17_15	P33	ARTIX1 DUT IO 173		
IO_L22N_T3_A16_15	P34	ARTIX1 DUT IO 174		
IO_L23P_T3_FOE_B_15	U24	ARTIX1 DUT IO 131		
IO_L23N_T3_FWE_B_15				
IO_L24P_T3_RS1_15				
IO_L24N_T3_RS0_15				
IO_25_15				

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A1_DUT_IO

BANK 16		U27E	L23	ARTIX1 DUT IO 115
		M24	ARTIX1 DUT IO 146	
IO_0_16	T24	ARTIX1 DUT IO 147		
IO_L1P_T0_16	K23	ARTIX1 DUT IO 132		
IO_L1N_T0_16	T23	ARTIX1 DUT IO 114		
IO_L2P_T0_16	G24	ARTIX1 DUT IO 129		
IO_L2N_T0_16	G25	ARTIX1 DUT IO 134		
IO_L3P_T0_DQS_16	K25	ARTIX1 DUT IO 142		
IO_L3N_T0_DQS_16	T25	ARTIX1 DUT IO 143		
IO_L4P_T0_16	M25	ARTIX1 DUT IO 118		
IO_L4N_T0_16	L25	ARTIX1 DUT IO 119		
IO_L5P_T0_16	T24	ARTIX1 DUT IO 116		
IO_L5N_T0_16	H24	ARTIX1 DUT IO 117		
IO_L6P_T0_16	H27	ARTIX1 DUT IO 103		
IO_L6N_T0_VREF_16	G27	ARTIX1 DUT IO 104		
IO_L7P_T1_16	H26	ARTIX1 DUT IO 101		
IO_L7N_T1_16	G26	ARTIX1 DUT IO 130		
IO_L8P_T1_16	T27	ARTIX1 DUT IO 122		
IO_L8N_T1_16	K27	ARTIX1 DUT IO 102		
IO_L9P_T1_DQS_16	K26	ARTIX1 DUT IO 49		
IO_L9N_T1_DQS_16	T26	ARTIX1 DUT IO 100		
IO_L10P_T1_16	L28	ARTIX1 DUT IO 140		
IO_L10N_T1_16	K28	ARTIX1 DUT IO 107		
IO_L11P_T1_SRCC_16	P28	ARTIX1 DUT IO 105		
IO_L11N_T1_SRCC_16	H28	ARTIX1 DUT IO 106		
IO_L12P_T1_MRCC_16	T29	ARTIX1 DUT IO 110		
IO_L12N_T1_MRCC_16	H29	ARTIX1 DUT IO 108		
IO_L13P_T2_MRCC_16	K30	ARTIX1 DUT IO 111		
IO_L13N_T2_MRCC_16	P30	ARTIX1 DUT IO 113		
IO_L14P_T2_SRCC_16	G29	ARTIX1 DUT IO 109		
IO_L14N_T2_SRCC_16	G30	ARTIX1 DUT IO 112		
IO_L15P_T2_DQS_16	K31	ARTIX1 DUT IO 152		
IO_L15N_T2_DQS_16	J31	ARTIX1 DUT IO 150		
IO_L16P_T2_16	H31	ARTIX1 DUT IO 180		
IO_L16N_T2_16	G31	ARTIX1 DUT IO 151		
IO_L17P_T2_16	T29	ARTIX1 DUT IO 125		
IO_L17N_T2_16	L30	ARTIX1 DUT IO 127		
IO_L18P_T2_16	H32	ARTIX1 DUT IO 154		
IO_L18N_T2_16	G32	ARTIX1 DUT IO 153		
IO_L19P_T3_16	K33	ARTIX1 DUT IO 186		
IO_L19N_T3_VREF_16	T34	ARTIX1 DUT IO 162		
IO_L20P_T3_16	H33	ARTIX1 DUT IO 160		
IO_L20N_T3_16	G34	ARTIX1 DUT IO 163		
IO_L21P_T3_DQS_16	L32	ARTIX1 DUT IO 156		
IO_L21N_T3_DQS_16	K32	ARTIX1 DUT IO 155		
IO_L22P_T3_16	T33	ARTIX1 DUT IO 170		
IO_L22N_T3_16	H34	ARTIX1 DUT IO 171		
IO_L23P_T3_16	J33	ARTIX1 DUT IO 169		
IO_L23N_T3_16	P34	ARTIX1 DUT IO 188		
IO_L24P_T3_16	M26	ARTIX1 DUT IO 121		
IO_L24N_T3_16				
IO_25_16				

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A

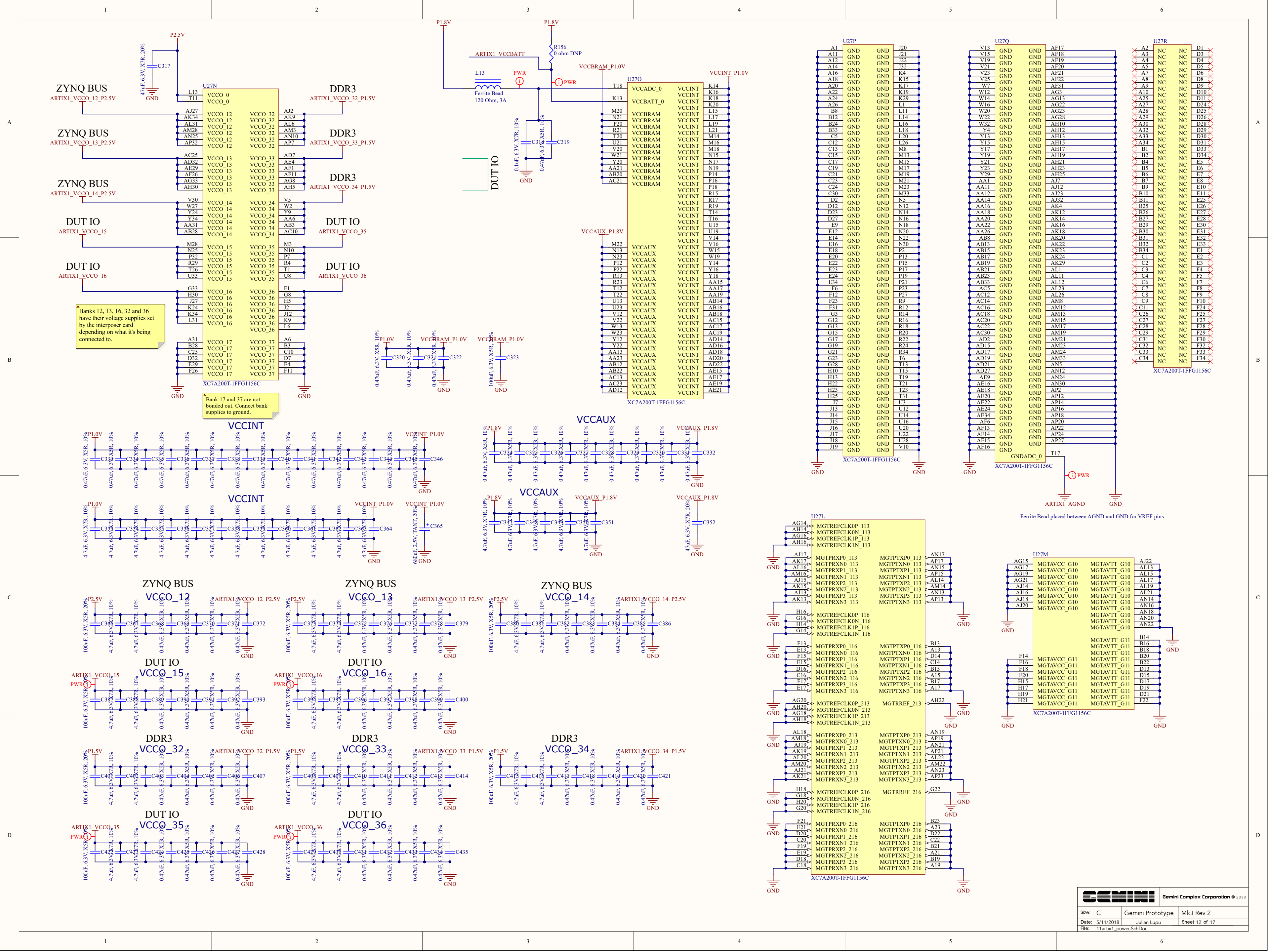
B

C

D

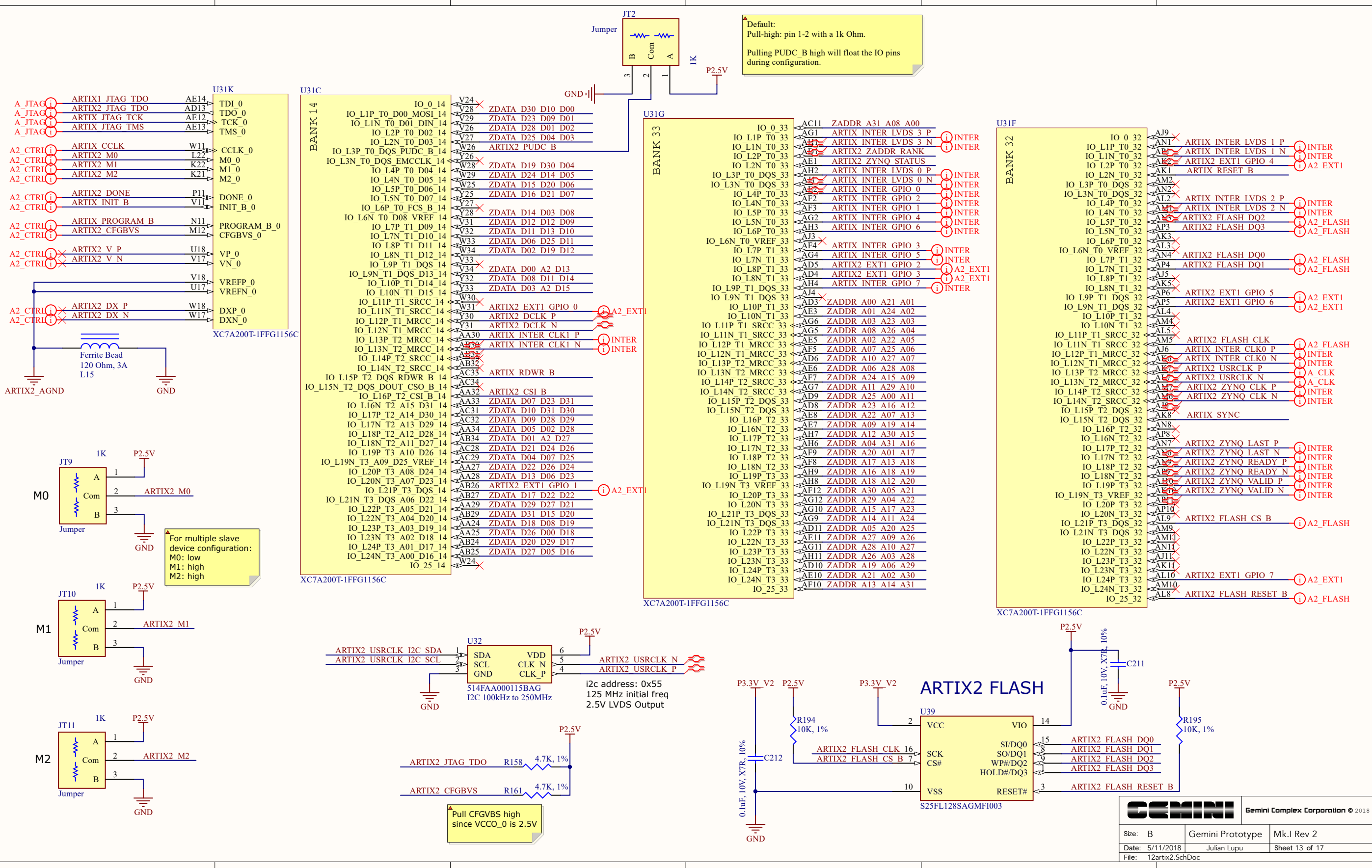
GEMINI Gemini Complex Corporation © 2018

Size: B	Gemini Prototype	Mk.I Rev 2
Date: 5/11/2018	Julian Lupu	Sheet 10 of 17
File: 09artix1_io.SchDoc		



Banks 12, 13, 16, 32 and 36 have their voltage supplies set by the interposer card depending on what it's being connected to.

Bank 17 and 37 are not bonded out. Connect bank supplies to ground.



		A2_DUT_IO	
U31D			
BANK 15			
IO 0_15 IO_L1P_T0_AD0P_15 IO_L1N_T0_AD0N_15 IO_L2P_T0_AD8P_15 IO_L2N_T0_AD8N_15 IO_L3P_T0_DQS_AD1P_15 IO_L3N_T0_DQS_AD1N_15 IO_L4P_T0_15 IO_L4N_T0_15 IO_L5P_T0_AD9P_15 IO_L5N_T0_AD9N_15 IO_L6P_T0_15 IO_L6N_T0_VREF_15 IO_L7P_T1_AD2P_15 IO_L7N_T1_AD2N_15 IO_L8P_T1_AD10P_15 IO_L8N_T1_AD10N_15 IO_L9P_T1_DQS_AD3P_15 IO_L9N_T1_DQS_AD3N_15 IO_L10P_T1_AD11P_15 IO_L10N_T1_AD11N_15 IO_L11P_T1_SRCC_15 IO_L11N_T1_SRCC_15 IO_L12P_T1_MRCC_15 IO_L12N_T1_MRCC_15 IO_L13P_T2_MRCC_15 IO_L13N_T2_MRCC_15 IO_L14P_T2_SRCC_15 IO_L14N_T2_SRCC_15 IO_L15P_T2_DQS_15 IO_L15N_T2_DQS_ADV_B_15 IO_L16P_T2_A28_15 IO_L16N_T2_A27_15 IO_L17P_T2_A26_15 IO_L17N_T2_A25_15 IO_L18P_T2_A24_15 IO_L18N_T2_A23_15 IO_L19P_T3_A22_15 IO_L19N_T3_A21_VREF_15 IO_L20P_T3_A20_15 IO_L20N_T3_A19_15 IO_L21P_T3_DQS_15 IO_L21N_T3_DQS_A18_15 IO_L22P_T3_A17_15 IO_L22N_T3_A16_15 IO_L23P_T3_FOE_B_15 IO_L23N_T3_FWE_B_15 IO_L24P_T3_RS1_15 IO_L24N_T3_RS0_15 IO_25_15	T24 ARTIX2 DUT IO 100 R26 ARTIX2 DUT IO 103 P26 ARTIX2 DUT IO 112 N26 ARTIX2 DUT IO 108 M27 ARTIX2 DUT IO 114 U25 ARTIX2 DUT IO 105 T25 ARTIX2 DUT IO 111 P24 ARTIX2 DUT IO 101 N24 ARTIX2 DUT IO 102 U26 ARTIX2 DUT IO 107 U27 ARTIX2 DUT IO 117 R25 ARTIX2 DUT IO 110 U25 ARTIX2 DUT IO 106 T27 ARTIX2 DUT IO 113 R27 ARTIX2 DUT IO 104 N27 ARTIX2 DUT IO 109 N28 ARTIX2 DUT IO 122 T28 ARTIX2 DUT IO 119 R28 ARTIX2 DUT IO 118 N29 ARTIX2 DUT IO 123 M29 ARTIX2 DUT IO 150 U29 ARTIX2 DUT IO 165 T29 ARTIX2 DUT IO 124 P28 ARTIX2 DUT IO 127 P29 ARTIX2 DUT IO 128 R30 ARTIX2 DUT IO 175 P30 ARTIX2 DUT IO 129 U30 ARTIX2 DUT IO 167 T30 ARTIX2 DUT IO 176 M30 ARTIX2 DUT IO 155 M31 ARTIX2 DUT IO 160 R31 ARTIX2 DUT IO 166 P31 ARTIX2 DUT IO 170 N31 ARTIX2 DUT IO 151 M32 ARTIX2 DUT IO 161 U31 ARTIX2 DUT IO 177 U32 ARTIX2 DUT IO 168 T32 ARTIX2 DUT IO 172 R32 ARTIX2 DUT IO 171 N32 ARTIX2 DUT IO 156 N33 ARTIX2 DUT IO 158 T33 ARTIX2 DUT IO 152 R33 ARTIX2 DUT IO 157 N34 ARTIX2 DUT IO 163 M34 ARTIX2 DUT IO 154 U34 ARTIX2 DUT IO 162 T34 ARTIX2 DUT IO 164 P33 ARTIX2 DUT IO 153 P34 ARTIX2 DUT IO 159 U24 ARTIX2 DUT IO 59		

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		A2_DUT_IO	
U31H			
BANK 34			
IO 0_34 IO_L1P_T0_34 IO_L1N_T0_34 IO_L2P_T0_34 IO_L2N_T0_34 IO_L3P_T0_DQS_34 IO_L3N_T0_DQS_34 IO_L4P_T0_34 IO_L4N_T0_34 IO_L5P_T0_34 IO_L5N_T0_34 IO_L6P_T0_34 IO_L6N_T0_VREF_34 IO_L7P_T1_34 IO_L7N_T1_34 IO_L8P_T1_34 IO_L8N_T1_34 IO_L9P_T1_DQS_34 IO_L9N_T1_DQS_34 IO_L10P_T1_34 IO_L10N_T1_34 IO_L11P_T1_SRCC_34 IO_L11N_T1_SRCC_34 IO_L12P_T1_MRCC_34 IO_L12N_T1_MRCC_34 IO_L13P_T2_MRCC_34 IO_L13N_T2_MRCC_34 IO_L14P_T2_SRCC_34 IO_L14N_T2_SRCC_34 IO_L15P_T2_DQS_34 IO_L15N_T2_DQS_34 IO_L16P_T2_34 IO_L16N_T2_34 IO_L17P_T2_34 IO_L17N_T2_34 IO_L18P_T2_34 IO_L18N_T2_34 IO_L19P_T3_34 IO_L19N_T3_VREF_34 IO_L20P_T3_34 IO_L20N_T3_34 IO_L21P_T3_DQS_34 IO_L21N_T3_DQS_34 IO_L22P_T3_34 IO_L22N_T3_34 IO_L23P_T3_34 IO_L23N_T3_34 IO_L24P_T3_34 IO_L24N_T3_34 IO_25_34	Y11 ARTIX2 DUT IO 121 W10 ARTIX2 DUT IO 134 Y10 ARTIX2 DUT IO 139 V9 ARTIX2 DUT IO 84 V8 ARTIX2 DUT IO 88 W9 ARTIX2 DUT IO 140 W8 ARTIX2 DUT IO 99 V7 ARTIX2 DUT IO 83 V6 ARTIX2 DUT IO 85 Y8 ARTIX2 DUT IO 89 Y7 ARTIX2 DUT IO 32 W6 ARTIX2 DUT IO 81 V6 ARTIX2 DUT IO 36 W1 ARTIX2 DUT IO 16 Y1 ARTIX2 DUT IO 25 V2 ARTIX2 DUT IO 28 V1 ARTIX2 DUT IO 26 V3 ARTIX2 DUT IO 24 Y2 ARTIX2 DUT IO 19 V3 ARTIX2 DUT IO 70 W3 ARTIX2 DUT IO 29 V4 ARTIX2 DUT IO 31 V4 ARTIX2 DUT IO 30 W5 ARTIX2 DUT IO 35 Y5 ARTIX2 DUT IO 47 AA5 ARTIX2 DUT IO 42 AA4 ARTIX2 DUT IO 46 AB5 ARTIX2 DUT IO 41 AB4 ARTIX2 DUT IO 45 AB2 ARTIX2 DUT IO 174 AB1 ARTIX2 DUT IO 185 AA3 ARTIX2 DUT IO 178 AA2 ARTIX2 DUT IO 195 AC2 ARTIX2 DUT IO 173 AC1 ARTIX2 DUT IO 190 AC4 ARTIX2 DUT IO 40 AC3 ARTIX2 DUT IO 179 AA8 ARTIX2 DUT IO 95 AA7 ARTIX2 DUT IO 49 AC7 ARTIX2 DUT IO 90 AC6 ARTIX2 DUT IO 43 AB7 ARTIX2 DUT IO 44 AB6 ARTIX2 DUT IO 48 AC9 ARTIX2 DUT IO 96 AC8 ARTIX2 DUT IO 91 AA10 ARTIX2 DUT IO 97 AA9 ARTIX2 DUT IO 92 AB10 ARTIX2 DUT IO 116 AB9 ARTIX2 DUT IO 125 AB11 ARTIX2 DUT IO 126		

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		A2_DUT_IO	
U31I			
BANK 35			
IO 0_35 IO_L1P_T0_AD4P_35 IO_L1N_T0_AD4N_35 IO_L2P_T0_AD12P_35 IO_L2N_T0_AD12N_35 IO_L3P_T0_DQS_AD5P_35 IO_L3N_T0_DQS_AD5N_35 IO_L4P_T0_35 IO_L4N_T0_35 IO_L5P_T0_AD13P_35 IO_L5N_T0_AD13N_35 IO_L6P_T0_35 IO_L6N_T0_VREF_35 IO_L7P_T1_AD6P_35 IO_L7N_T1_AD6N_35 IO_L8P_T1_AD14P_35 IO_L8N_T1_AD14N_35 IO_L9P_T1_DQS_AD7P_35 IO_L9N_T1_DQS_AD7N_35 IO_L10P_T1_AD15P_35 IO_L10N_T1_AD15N_35 IO_L11P_T1_SRCC_35 IO_L11N_T1_SRCC_35 IO_L12P_T1_MRCC_35 IO_L12N_T1_MRCC_35 IO_L13P_T2_MRCC_35 IO_L13N_T2_MRCC_35 IO_L14P_T2_SRCC_35 IO_L14N_T2_SRCC_35 IO_L15P_T2_DQS_35 IO_L15N_T2_DQS_35 IO_L16P_T2_35 IO_L16N_T2_35 IO_L17P_T2_35 IO_L17N_T2_35 IO_L18P_T2_35 IO_L18N_T2_35 IO_L19P_T3_35 IO_L19N_T3_VREF_35 IO_L20P_T3_35 IO_L20N_T3_35 IO_L21P_T3_DQS_35 IO_L21N_T3_DQS_35 IO_L22P_T3_35 IO_L22N_T3_35 IO_L23P_T3_35 IO_L23N_T3_35 IO_L24P_T3_35 IO_L24N_T3_35 IO_25_35	R11 ARTIX2 DUT IO 138 M7 ARTIX2 DUT IO 73 M6 ARTIX2 DUT IO 67 N9 ARTIX2 DUT IO 137 M9 ARTIX2 DUT IO 74 N8 ARTIX2 DUT IO 147 N7 ARTIX2 DUT IO 136 M11 ARTIX2 DUT IO 54 M10 ARTIX2 DUT IO 120 P9 ARTIX2 DUT IO 132 P8 ARTIX2 DUT IO 142 P6 ARTIX2 DUT IO 141 N6 ARTIX2 DUT IO 146 N1 ARTIX2 DUT IO 192 M1 ARTIX2 DUT IO 180 V5 ARTIX2 DUT IO 71 M4 ARTIX2 DUT IO 75 P1 ARTIX2 DUT IO 194 R1 ARTIX2 DUT IO 193 N3 ARTIX2 DUT IO 187 W2 ARTIX2 DUT IO 18 P4 ARTIX2 DUT IO 188 R3 ARTIX2 DUT IO 186 P5 ARTIX2 DUT IO 135 N4 ARTIX2 DUT IO 145 R6 ARTIX2 DUT IO 80 R5 ARTIX2 DUT IO 130 T5 ARTIX2 DUT IO 34 T4 ARTIX2 DUT IO 33 R3 ARTIX2 DUT IO 189 R2 ARTIX2 DUT IO 199 U2 ARTIX2 DUT IO 17 U1 ARTIX2 DUT IO 21 T3 ARTIX2 DUT IO 183 T2 ARTIX2 DUT IO 23 U5 ARTIX2 DUT IO 38 U4 ARTIX2 DUT IO 37 R8 ARTIX2 DUT IO 87 R7 ARTIX2 DUT IO 131 R10 ARTIX2 DUT IO 133 P10 ARTIX2 DUT IO 148 U10 ARTIX2 DUT IO 144 T10 ARTIX2 DUT IO 143 U7 ARTIX2 DUT IO 82 U6 ARTIX2 DUT IO 39 T8 ARTIX2 DUT IO 93 T7 ARTIX2 DUT IO 86 U9 ARTIX2 DUT IO 94 T9 ARTIX2 DUT IO 98 U11 ARTIX2 DUT IO 149		

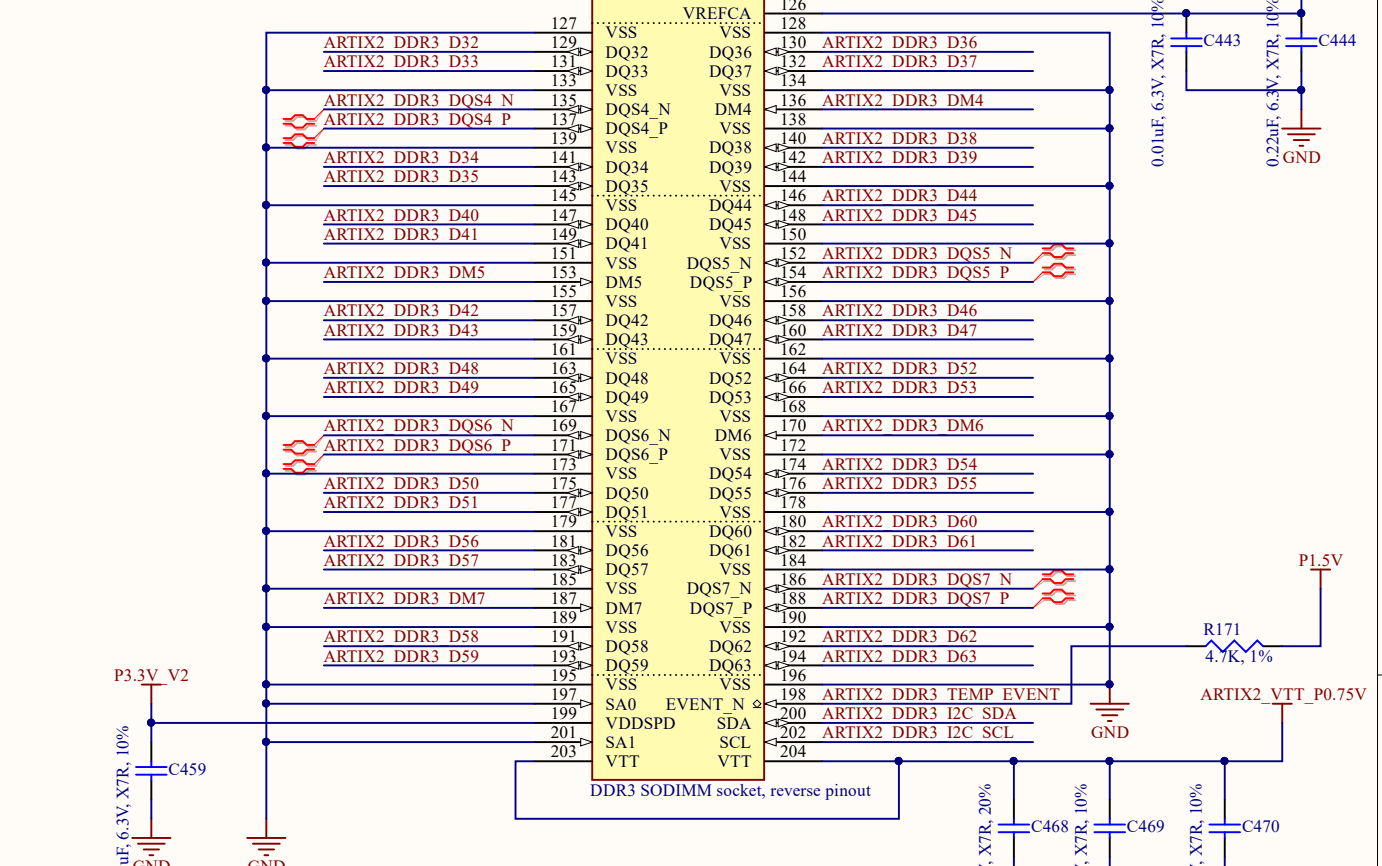
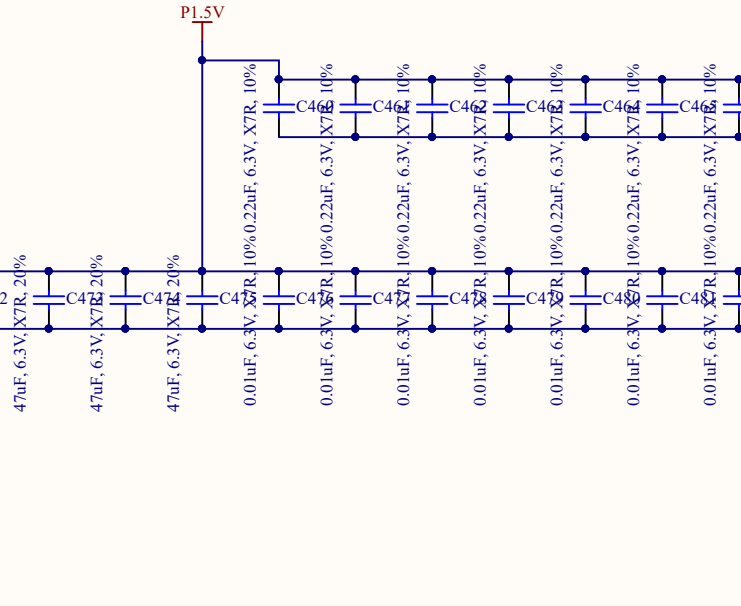
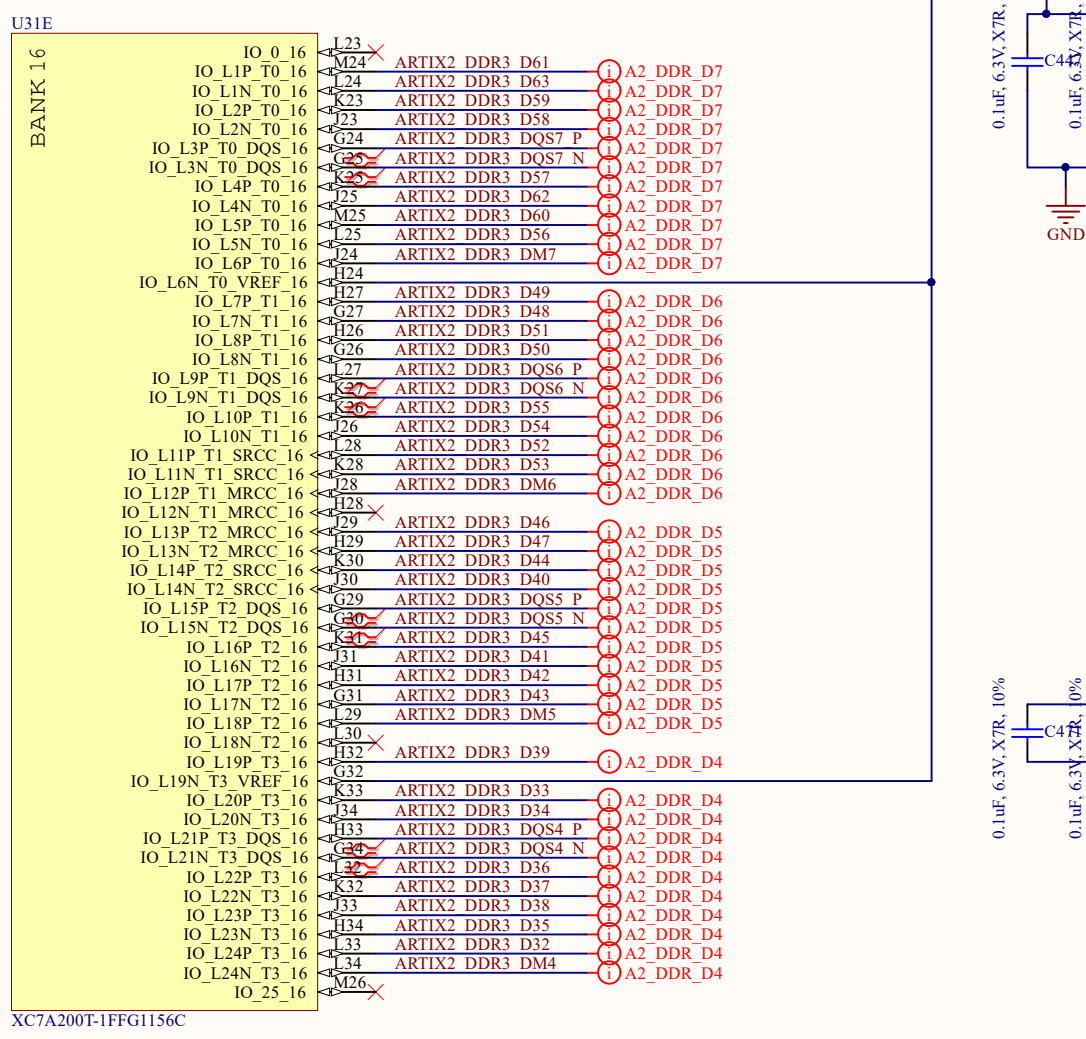
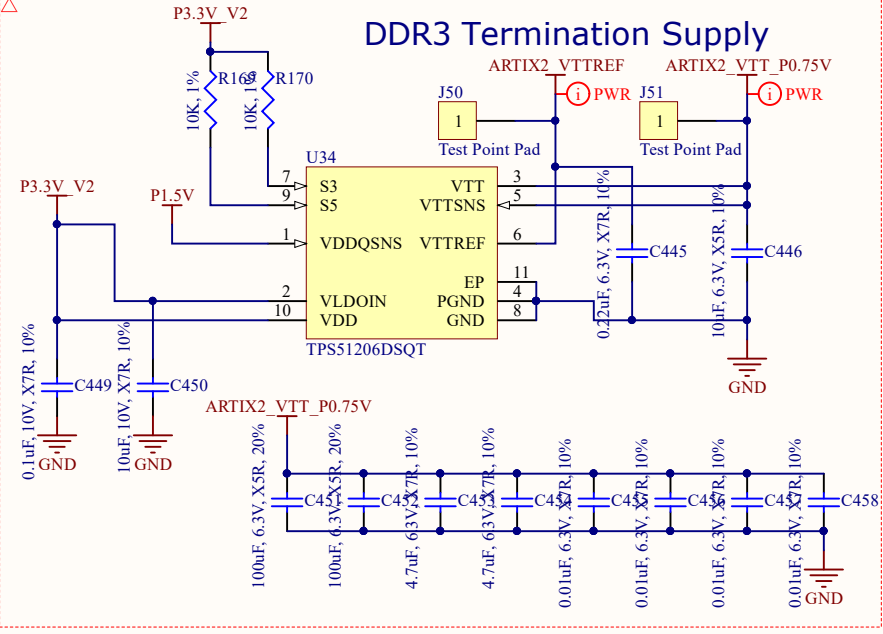
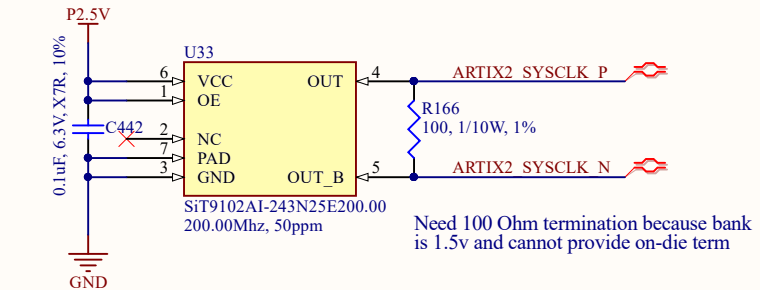
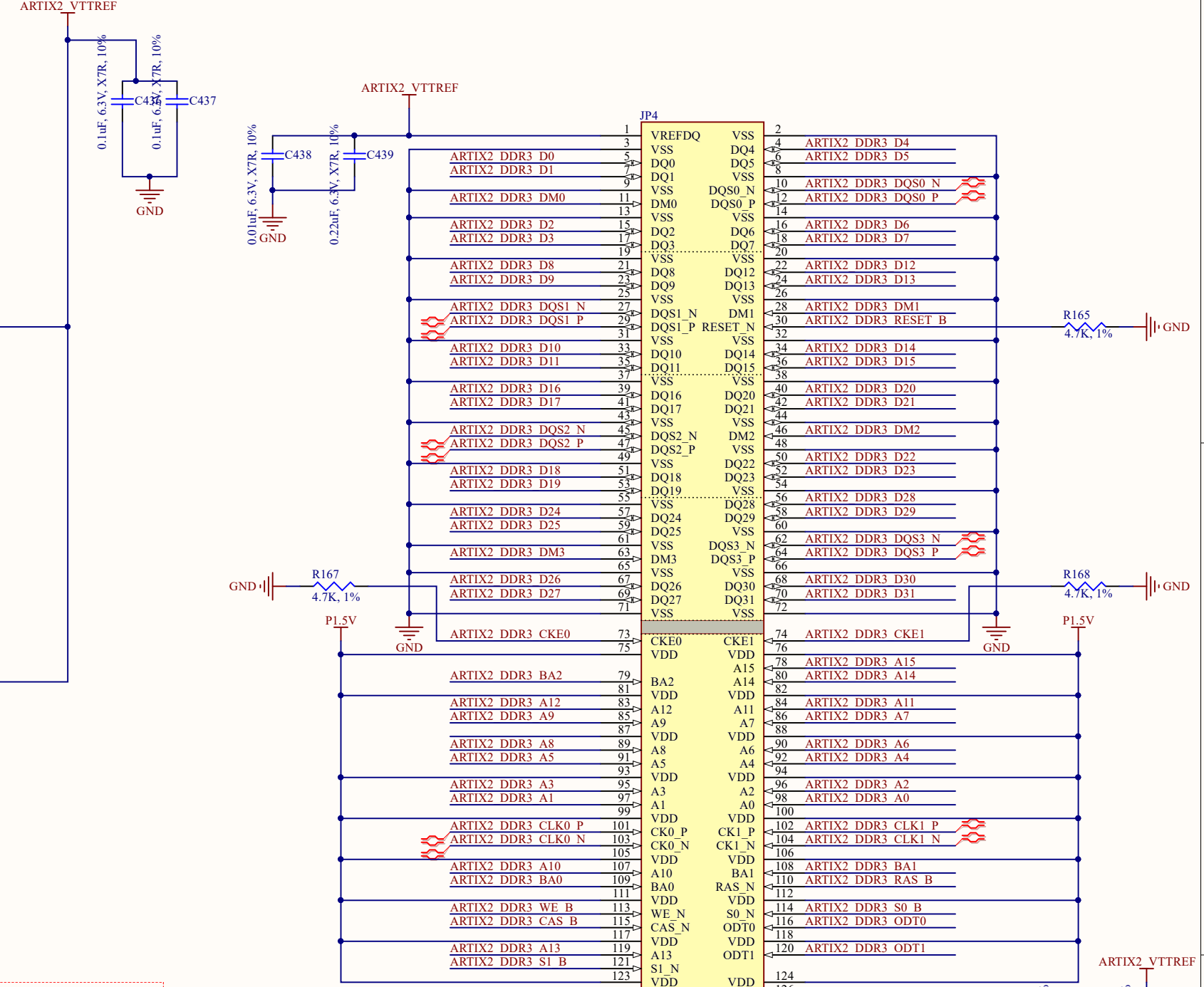
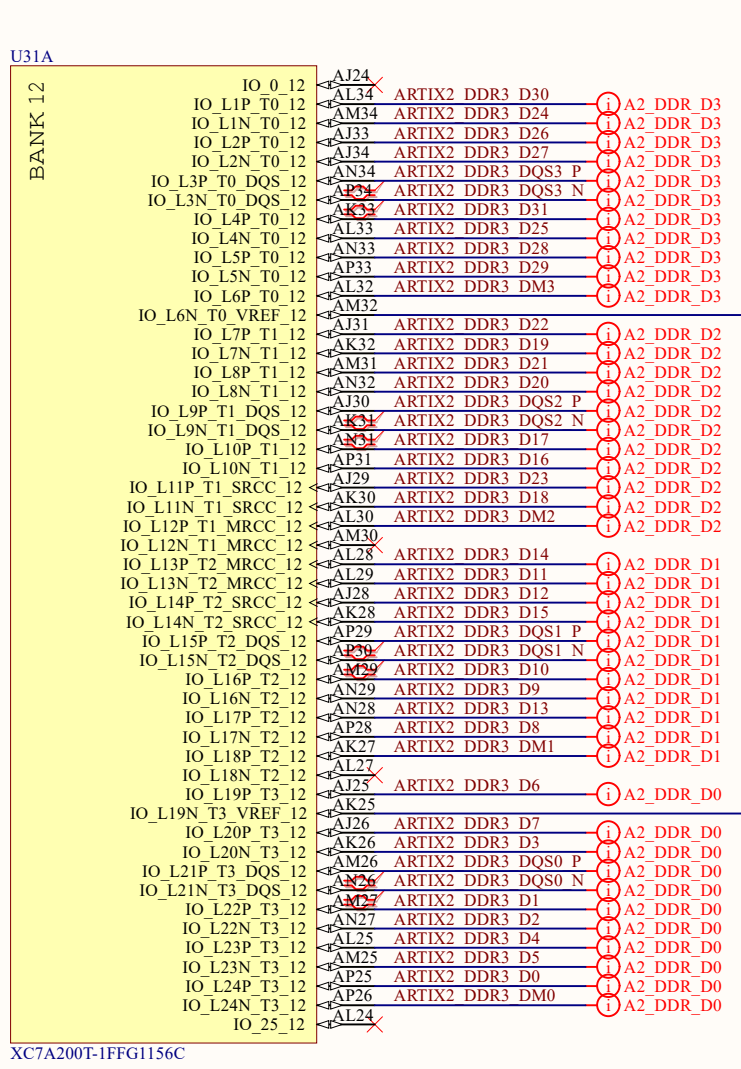
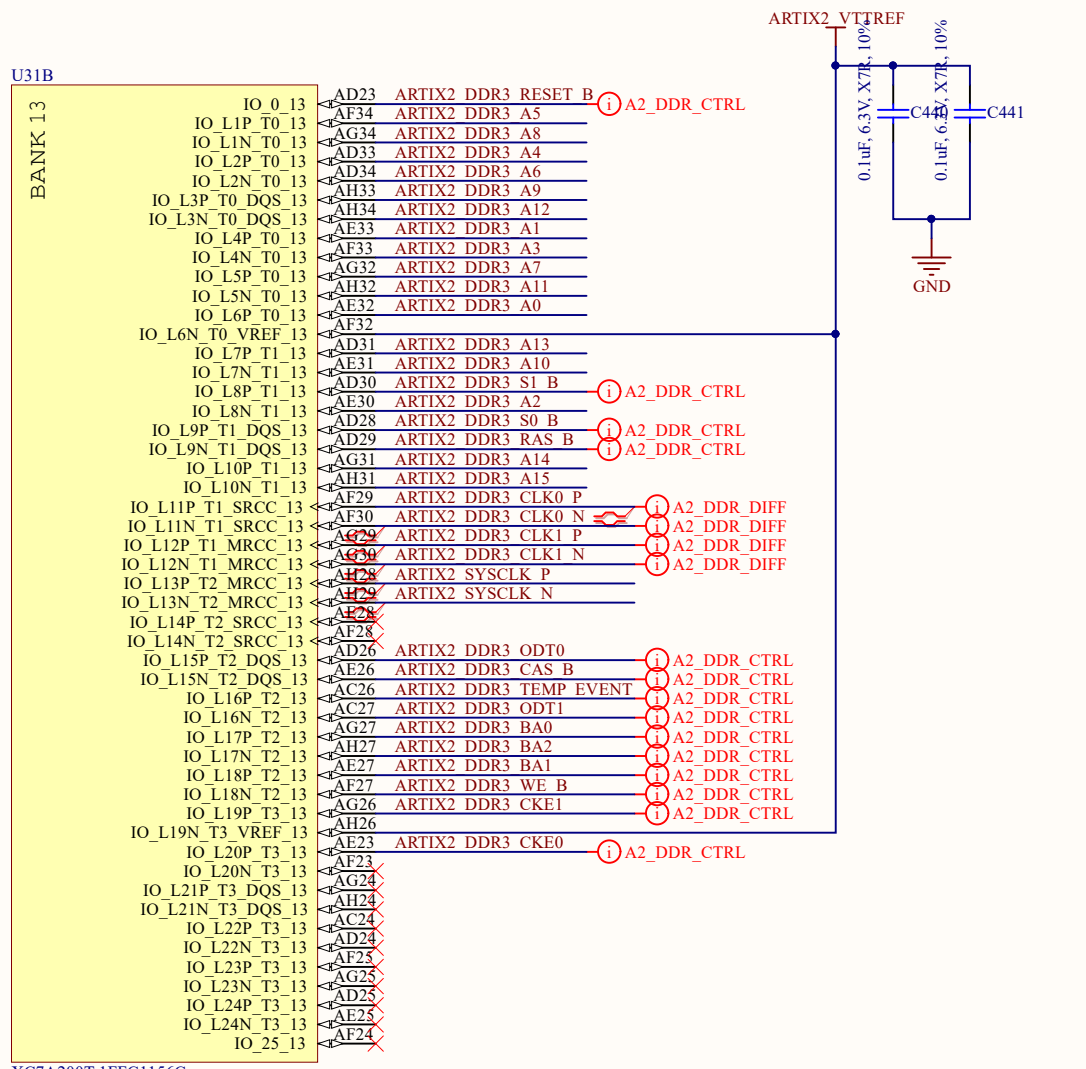
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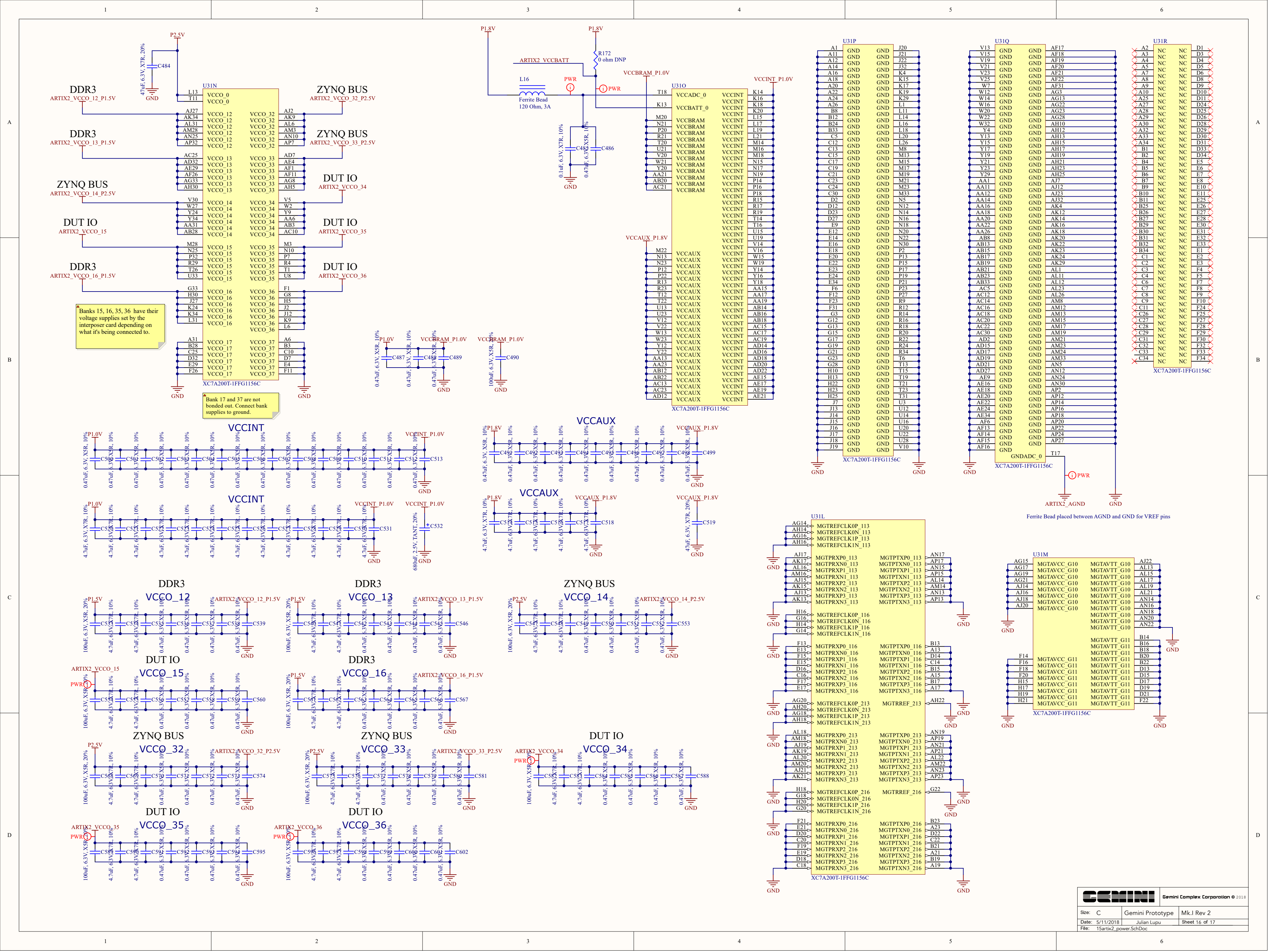
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U31J			
BANK 36			
IO 0_36 IO_L1P_T0_36 IO_L1N_T0_36 IO_L2P_T0_36 IO_L2N_T0_36 IO_L3P_T0_DQS_36 IO_L3N_T0_DQS_36 IO_L4P_T0_36 IO_L4N_T0_36 IO_L5P_T0_36 IO_L5N_T0_36 IO_L6P_T0_36 IO_L6N_T0_VREF_36 IO_L7P_T1_36 IO_L7N_T1_36 IO_L8P_T1_36 IO_L8N_T1_36 IO_L9P_T1_DQS_36 IO_L9N_T1_DQS_36 IO_L10P_T1_36 IO_L10N_T1_36 IO_L11P_T1_SRCC_36 IO_L11N_T1_SRCC_36 IO_L12P_T1_MRCC_36 IO_L12N_T1_MRCC_36 IO_L13P_T2_MRCC_36 IO_L13N_T2_MRCC_36 IO_L14P_T2_SRCC_36 IO_L14N_T2_SRCC_36 IO_L15P_T2_DQS_36 IO_L15N_T2_DQS_36 IO_L16P_T2_36 IO_L16N_T2_36 IO_L17P_T2_36 IO_L17N_T2_36 IO_L18P_T2_36 IO_L18N_T2_36 IO_L19P_T3_36 IO_L19N_T3_VREF_36 IO_L20P_T3_36 IO_L20N_T3_36 IO_L21P_T3_DQS_36 IO_L21N_T3_DQS_36 IO_L22P_T3_36 IO_L22N_T3_36 IO_L23P_T3_36 IO_L23N_T3_36 IO_L24P_T3_36 IO_L24N_T3_36 IO_25_36	H12 ARTIX2 DUT IO 53 K12 ARTIX2 DUT IO 64 K12 ARTIX2 DUT IO 58 G10 ARTIX2 DUT IO 56 G9 ARTIX2 DUT IO 55 K11 ARTIX2 DUT IO 63 H11 ARTIX2 DUT IO 57 H11 ARTIX2 DUT IO 62 G11 ARTIX2 DUT IO 52 L10 ARTIX2 DUT IO 115 L9 ARTIX2 DUT IO 79 K10 ARTIX2 DUT IO 61 H10 ARTIX2 DUT IO 51 L9 ARTIX2 DUT IO 65 H8 ARTIX2 DUT IO 4 H9 ARTIX2 DUT IO 50 H8 ARTIX2 DUT IO 60 K8 ARTIX2 DUT IO 78 K8 ARTIX2 DUT IO 69 G7 ARTIX2 DUT IO 9 G6 ARTIX2 DUT IO 8 K7 ARTIX2 DUT IO 68 K6 ARTIX2 DUT IO 72 K7 ARTIX2 DUT IO 3 H6 ARTIX2 DUT IO 2 G5 ARTIX2 DUT IO 13 G4 ARTIX2 DUT IO 12 L6 ARTIX2 DUT IO 14 L5 ARTIX2 DUT IO 7 F3 ARTIX2 DUT IO 11 F2 ARTIX2 DUT IO 181 L5 ARTIX2 DUT IO 76 K5 ARTIX2 DUT IO 1 H4 ARTIX2 DUT IO 6 H3 ARTIX2 DUT IO 5 L4 ARTIX2 DUT IO 0 L4 ARTIX2 DUT IO 20 L3 ARTIX2 DUT IO 66 L3 ARTIX2 DUT IO 10 H2 ARTIX2 DUT IO 191 G2 ARTIX2 DUT IO 182 K1 ARTIX2 DUT IO 196 H1 ARTIX2 DUT IO 169 H1 ARTIX2 DUT IO 184 G1 ARTIX2 DUT IO 197 M2 ARTIX2 DUT IO 27 L2 ARTIX2 DUT IO 22 K3 ARTIX2 DUT IO 15 K2 ARTIX2 DUT IO 198 L7 ARTIX2 DUT IO 77		

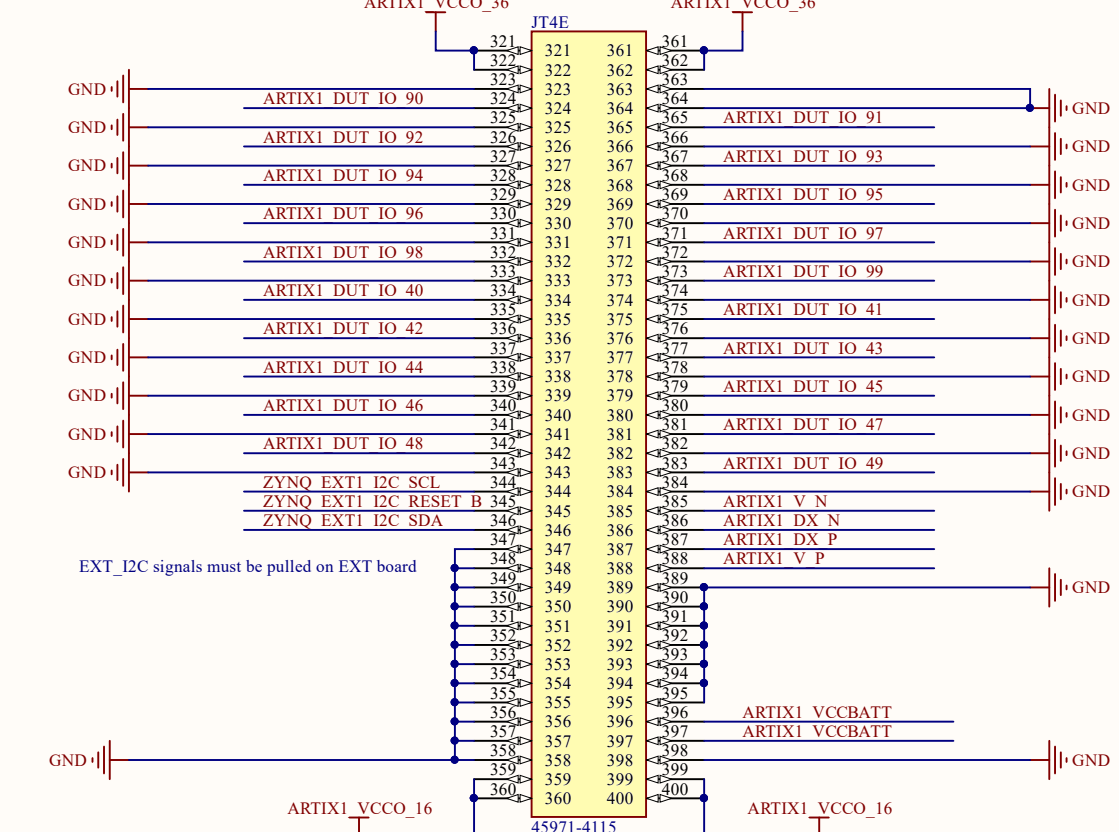
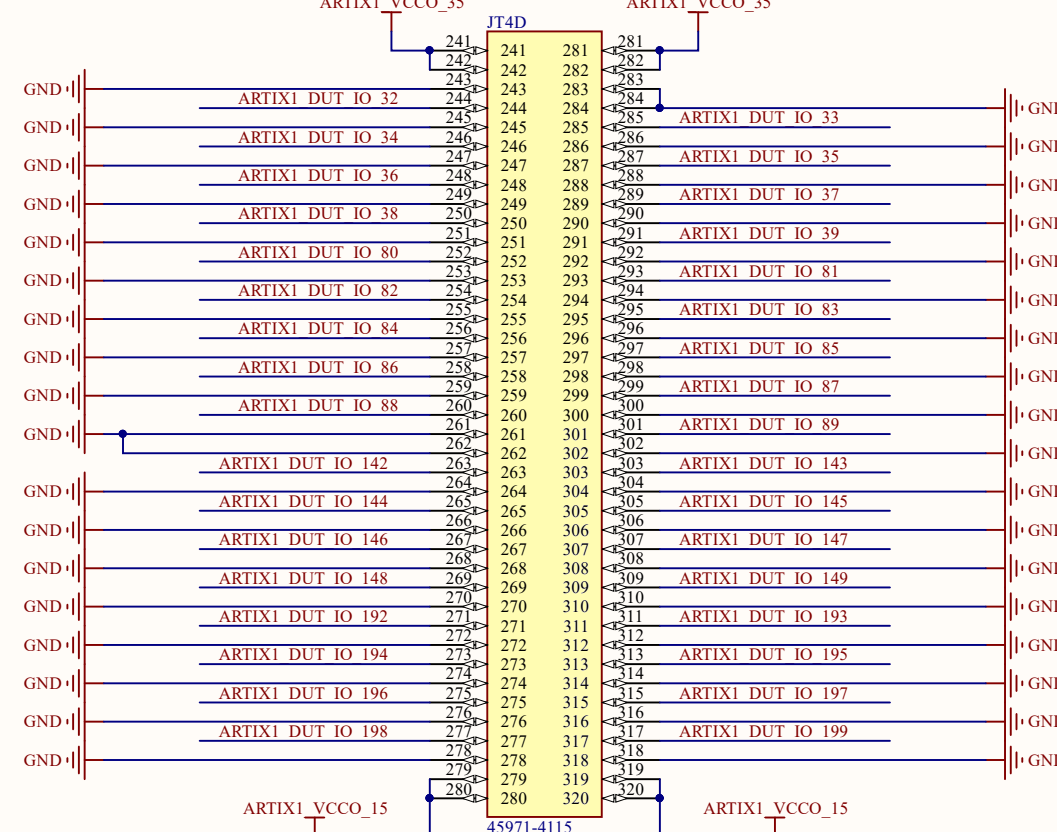
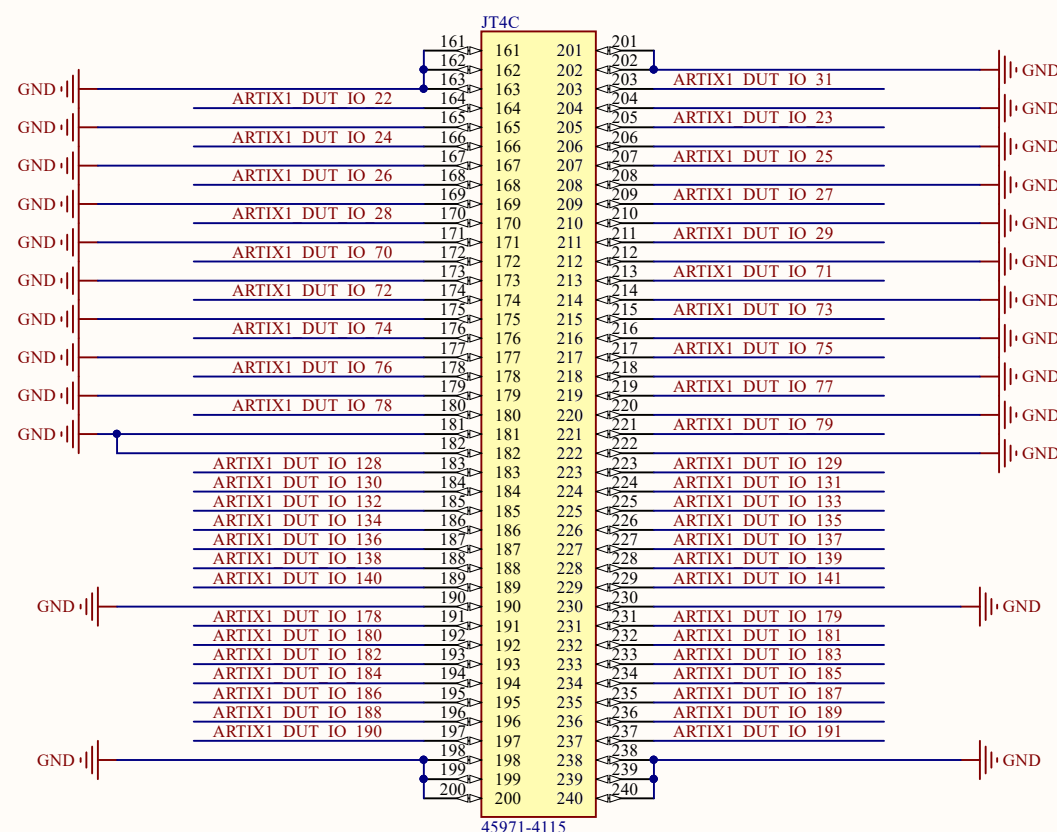
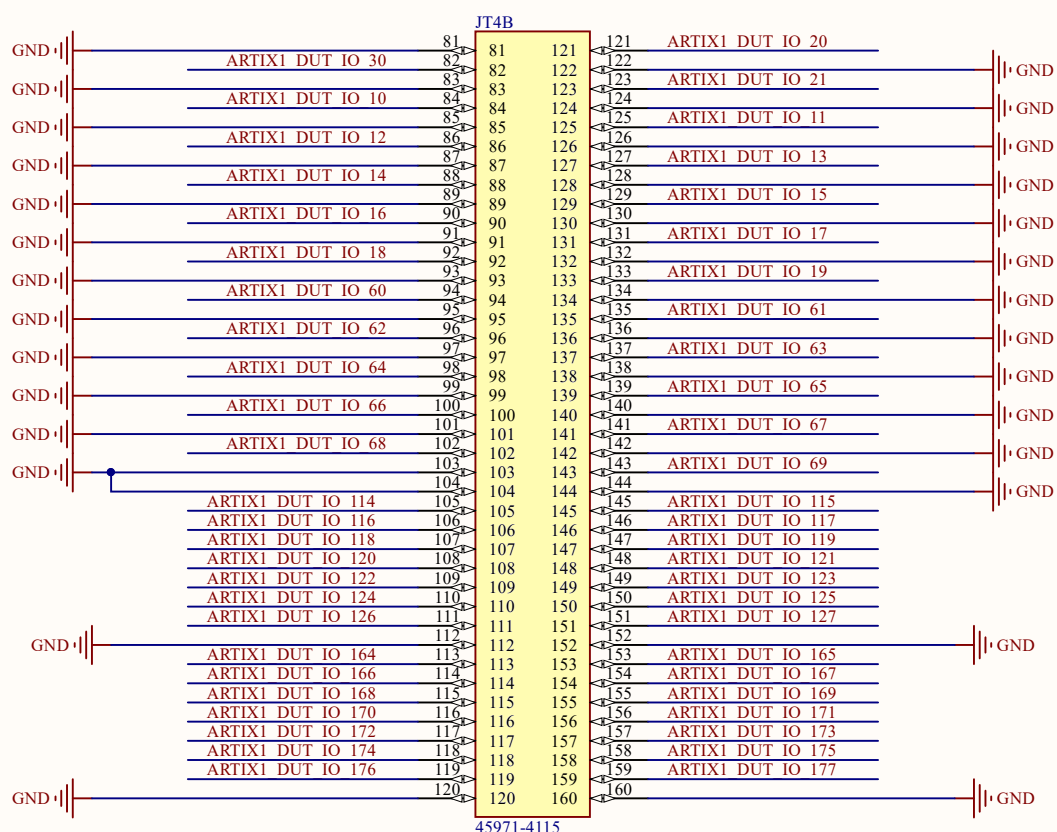
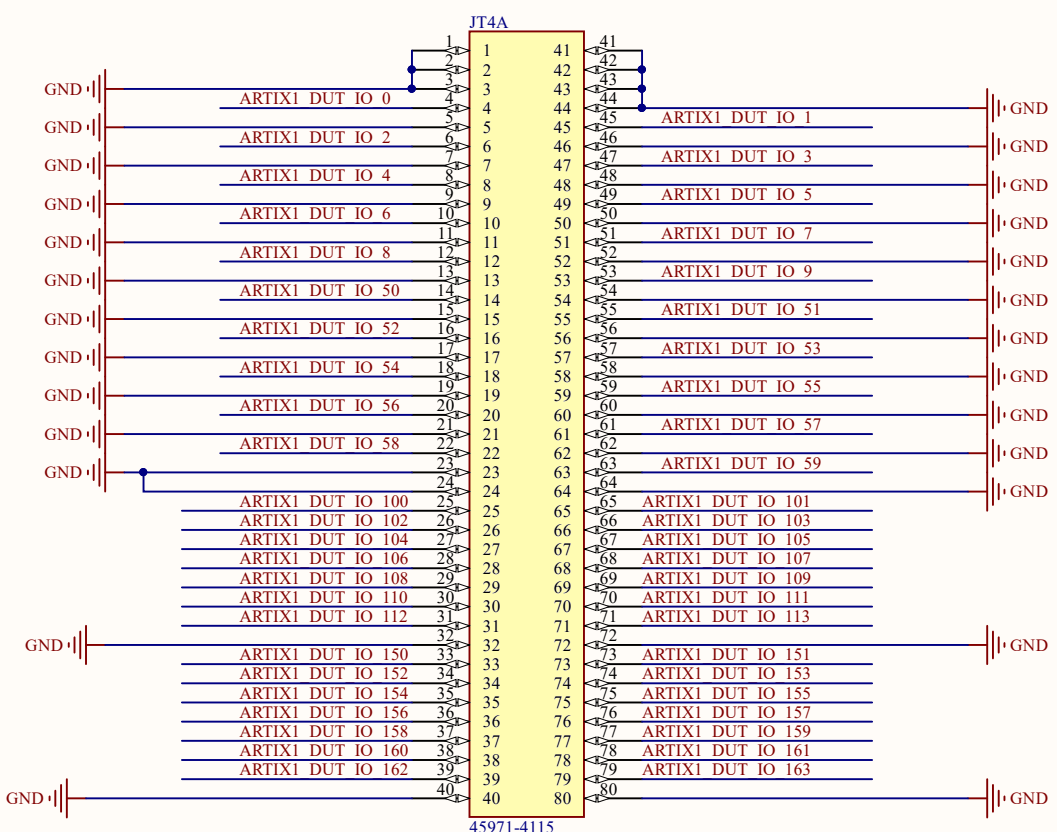
XC7A200T-1FFG1156C

Bank 34 pins operate at 1.5v. We need to communicate between artix units so we use remaining pins to do that. These can be used to pass data and to sync units when driving/reading DUT.

ARTIX2_DDR3_A[0..15] A2_DDR_ADDRESS
 ARTIX2_DDR3_D[0..63] A2_DDR_DATA
 ARTIX2_DDR3_DM[0..7] A2_DDR_MASK







RESET NOTE:
 If the EXT1 peripheral wants to reset it must assert EXT1_ZYNQ_SRST_B.
 If it wants to check the state of reset, it should read ZYNQ_RESET_B, but never drive it.
 Both are 3.3V signals.

