Gemini Mk.I Tester Platform

Features

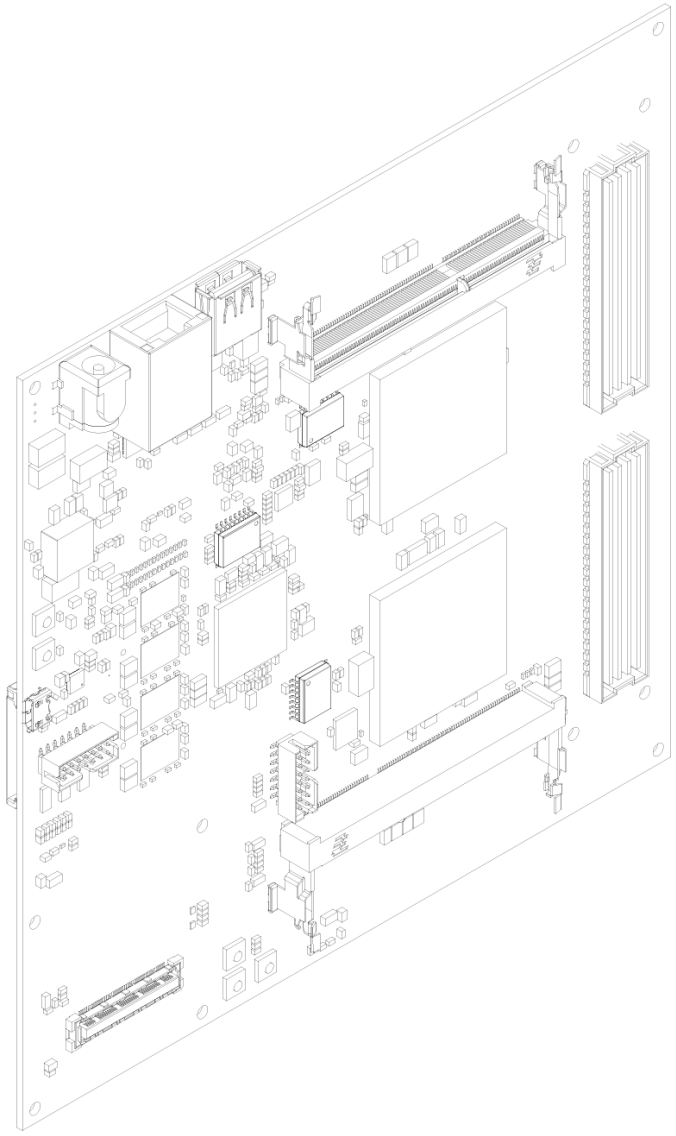
- VecOS™ Test Execution Engine
- Dual Vector Engines
- Solo or Synced Test Mode
- 400 Pin DUT I/O Test Bus
- 50MHz Vector Execution Speed
- 67M Deep Vector Burst†
- 20 Gbps continuous data bandwidth‡
- Test Pattern Loading Over NFS
- Gigabit Ethernet Interface
- USB Interface
- SD Card Interface
- Modular DUT Board Interface
- Frontend Web GUI
- HTTP Based API
- Python Module API
- Simple Test Pattern Language
- High-Performance Test Pattern Binary Compiler

Description

The Gemini Mk.I Tester Platform is a high-speed digital functional tester designed to operate in either a standalone or integrated mode. The system is designed to interface with single and multi-site DUT (Device-Under-Test) boards through two high-density DUT Expansion Ports. The platform comes preinstalled with VecOS™, a software operating system responsible for managing, queuing and executing test programs and pre-compiled test pattern binaries, serving APIs and GUI frontends, and reporting test program statistics.

† The true tester vector depth is 67,108,864 vectors. The definition of "burst execution" is continuous execution without memory stalls. The Vector Engines can execute a 67M vector burst if using clocked vectors. Please see Vector Engine section for more information.

‡ The continuous data bandwidth value only applies when running a dual-mode test pattern and is calculated by taking the number of DUT I/O test pins over the Vector Engine T_{vec} period.



1 Physical Description

The Gemini board is a small form-factor, miniaturized ATE (Automatic Test Equipment) test platform, designed to be modular and seamlessly integrate into larger systems through the DUT Expansion Port interface. It comes equipped with powerful processor compute units to deliver uncompromised performance as well as multiple peripheral interfaces offering greater flexibility.

- Xilinx Zynq-7000 SoC
  - Arm Cortex-A9 Dual-Core CPU
  - Artix-7 FPGA Logic
  - Gigabit Ethernet
  - USB 2.0
  - SD Card MMC
  - Runs VecOS™
- 2x Xilinx Artix-7 FPGAs
  - 2x 8GB DDR3 204 Pin SODIMM RAM
  - Dual Vector Engines
- Power Management System
- 2x 400 Pin Board-to-Board DUT Expansion Ports (industry standard I/O)
  - DUT I/O Test Bus (2x 200)
  - Control, Status and I^2C Signals
  - Power
- High-Speed Expansion Port
  - Reserved for Future Use

2 Functional Description

2.1 Functional Testing Overview

The Gemini board is designed to functionally test digital logic devices through the board-to-board DUT Expansion Ports, given that the external DUT board conforms to the physical and electrical interface specifications. Test engineers can design test patterns using a simple text-file based language called Dots, to arbitrarily test attached DUTs (Device-Under-Test) through the DUT I/O test bus. A test pattern consists of a list of test vectors which, given a set of pre-defined test pins, will digitally drive pins and expect logic values per test cycle, as specified by the test engineer. Test vectors that expect different logic values than stated for a given vector will fail. If a test pattern fails, the failing cycle count and the failing pins will be returned by VecOS™. Test pattern Dots files are compiled to proprietary binary files called *stim* files. Test patterns are compiled using a pin-mapping file called a *profile* file, which corresponds to the DUT board's netlist. The purpose of a profile is to let the compiler know how test pins map to the DUT I/O test bus. To test a group of test patterns sequentially, a text-based file known as a test program must be created. VecOS™, the Gemini test execution operating system, handles queuing and loading of test programs and test pattern binaries into tester memory, executing the tests and reporting the status. Please see the Gemini User Guide for more information.

2.2 Vector Engine

The Gemini board comes equipped with two test pattern execution engines, called Vector Engines, which are part of VecOS™. The two Vector Engines are located within each Xilinx Artix-7 FPGA unit. Each Vector Engine has access to 200 pins of the total 400 pin DUT I/O test bus. The Vector Engine is responsible for loading test patterns into tester memory, reading from tester memory, executing test vectors, returning a test pass or fail status message, cycle count, and which DUT I/O pins failed, if the test failed. The default behavior of a test pattern that fails is to stop driving or expecting once it fails.

Test patterns can run in solo-mode or dual-mode. In solo-mode, patterns can run on either Vector Engine, independently of the other Vector Engine. In dual-mode, test patterns run on both Vector Engines in sync and have access to the full tester memory available to both Vector Engines. A test pattern's mode is not set manually but is set based on which DUT I/O test pins it uses. If the test pattern uses DUT I/O pins from both Vector Engines, the test pattern compiler will automatically set the compiled pattern to dual-mode. If the test pattern only uses DUT I/O pins from one Vector Engine, it will automatically get set to solo-mode. Obviously if running a dual-mode pattern, both Vector Engines will be occupied, and no solo-mode patterns can run until the test has finished. Test engineers need to be aware of this when creating test programs.

Table 1 – Vector Engine Characteristics

Symbol	Description	Min	Nom	Max	Unit
f_{vec}	Vector Execution Frequency	–	–	50	MHz
T_{vec}	Vector Execution Period	–	–	20	ns
D_{vec} (1)	Vector Burst Depth	–	–	67,108,864 (2) (3)	Count
M_{vec}	Vector Memory	–	–	8,589,934,592/17,179,869,184(4)	Bytes

Notes:

1. Vectors can toggle a clock by using a special Dots drive value of "C". This value is the number of clocked vectors, with no repeat value, that can be burst executed without stalling.
2. Test patterns with no clocked vectors or repeats can temporarily stall after 37,008 cycles. When a stall occurs, the engine stops driving (high-Z output) or expecting until vectors, from memory, are available again.
3. Each Vector Engine can load 67,108,864, 200-pin test vectors into its tester memory.
4. Each Vector Engine has 8GiB of tester memory or combined total of 16GiB for both Vector Engines. In dual-mode, each Vector Engine will read vectors from its own tester memory and execute the vectors in sync.

2.3 Vector Timing

Test pattern vectors compile down to vector primitives, each with specific timing characteristics. Each of the varying primitives, seen in the table below, are packed into one binary test vector. VecOS™ handles loading of the binary test vectors into tester memory and starts the test. The Vector Engines then receive a test vector every T_{vec} clock cycle, given that no stalls occur, and execute the vector either by driving or expecting. If executing a multi-cycle vector, the Vector Engine will continue to buffer vectors while the current vector is being executed. When all the test vector cycles finish executing, the test is finished.

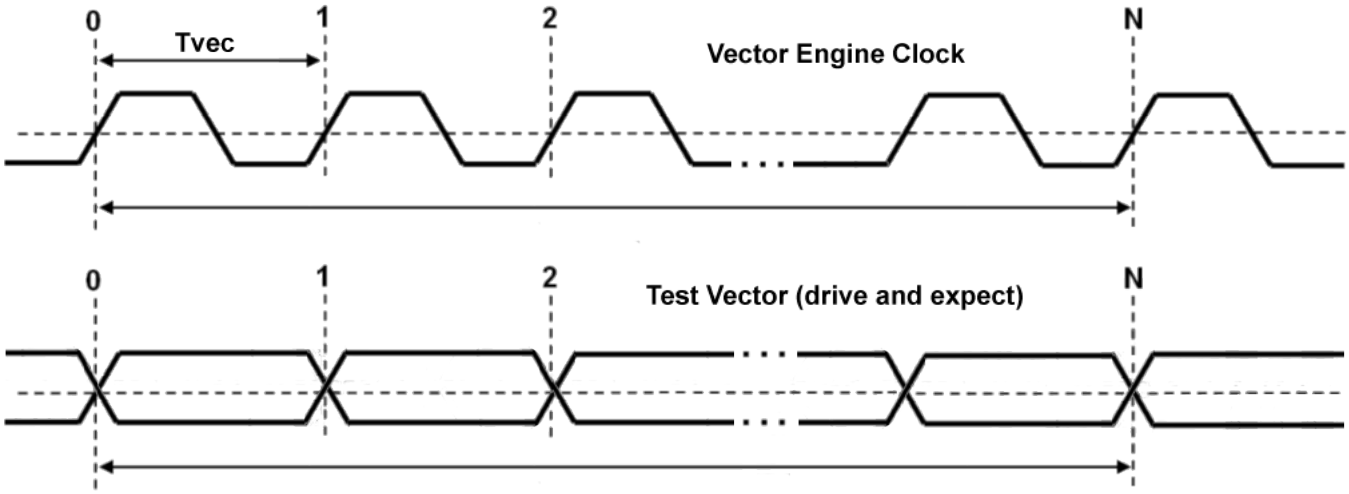
Table 2 – Vector Primitives

Type	Description	Cycles (1)(2)
VEC	Single cycle vector with no repeat	1
VEC_LOOP	Looped vector based on repeat value	N
VEC_CLK (3)	Clocked vector with optional repeat value	(N * 2)

Notes:

1. Cycles refers to the number of T_{vec} Vector Engine clock cycles.
2. N refers to number of cycles based on the repeat value used. N cannot be less than or equal to zero. N cannot be greater than 137,438,953,472 cycles. It is not recommended for N to exceed 34,359,738,368 cycles; however, it is allowed.
3. The Vector Engine internally expands VEC_CLK into two VEC vectors (multiplied by the repeat value) and drives the pins with a Dots drive value of "C" low and then high.

Figure 1 – Vector Engine Timing Diagram



3 Power, System and Interface Descriptions

3.1 Board Power

The Gemini board was designed to operate in either a standalone desktop mode or in a system integrated mode. Functionally there is no difference between the two modes. The main difference is the way the Gemini board is powered. Power is provided either through the DC power jack or through the DUT board's expansion port. All on-board voltage rails are generated from either power input, except the DUT I/O V_{CCO} rails, which must be correctly generated on the DUT board.

Important note: The required electrical specifications detailed in the Physical/Electrical Characteristics sections must be met for correct operation.

Table 3 - Board Power Inputs

Name	Type	Description
PWR_JACK	Power Input	DC power jack input
PWR_DUT	Power Input / Output	DUT board power pins

Important note*:* the board must not be powered through both the DC power jack (PWR_JACK) and the expansion port (PWR_DUT) at the same time. Doing so can permanently damage the board.

3.1.1 DC Power Jack – PWR_JACK

Normally, the Gemini board will be powered through the DC power jack if operating in standalone mode. If the board is powered through the DC power jack (PWR_JACK), the board will output a filtered PWR_DUT rail for the DUT board to utilize and further generate needed rails from, given that it meets the electrical requirements. However, the power supply used to power PWR_JACK, must be capable of delivering the necessary power for both the Gemini board and the DUT board. If the PWR_JACK power supply cannot deliver the required power for both boards, the DUT board must be powered separately.

Table 4 – DC Power Jack Component

Description	Part Number	Manufacturer
Connector Power Jack 2.1X5.5mm	PJ-002AH-SMT-TR	CUI

3.1.2 DUT Expansion Port Power Pins – PWR_DUT

If the Gemini board is operating in an integrated mode, it is highly recommended that the Gemini board be powered through the DUT Expansion Port's PWR_DUT pins, with an adequate and properly filtered voltage supply rail.

Figure 2 - PWR_DUT Filtering Example Circuit

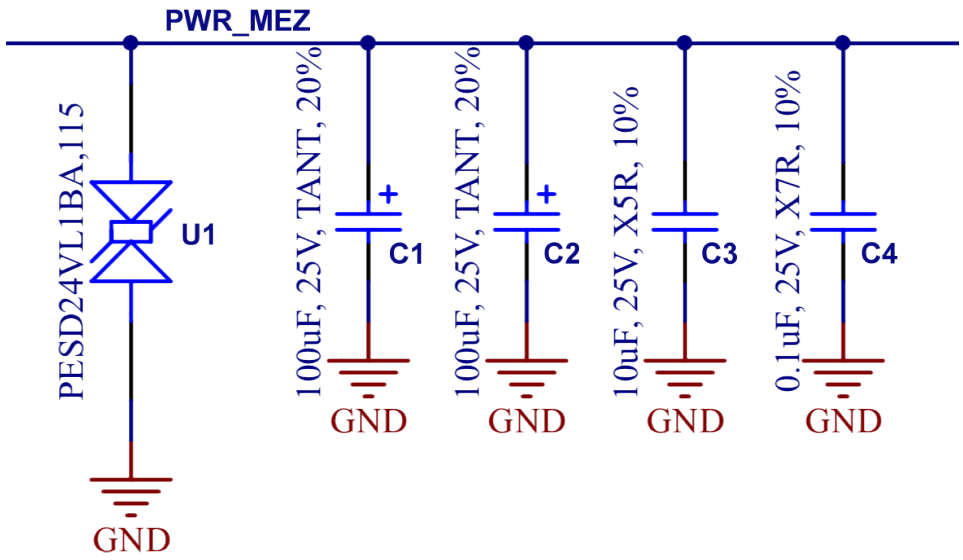


Table 5 – PWR_DUT Filtering Circuit Component Recommendation (1)

Reference	Description	Part Number	Manufacturer
U1	TVS DIODE 24VWM 70VC SOD323	PESD24VL1BA,115	Texas Instruments
C1	CAP TANT POLY 100UF 25V 20% 2917	TCJE107M025R0080	AVX
C2	CAP TANT POLY 47UF 25V 20% 2917	TCNX476M025R0100	AVX
C3	CAP CER 10UF 25V X5R 10% 0805	C2012X5R1V106K125AC	Murata
C4	CAP CER 0.1UF 25V X7R 10% 0603	GRM188R71E104KA01D	Murata

Notes:

1. See *Third-Party Products* Disclaimer

Important note: The Gemini board does not have a polarity protection diode on PWR_DUT because it is bidirectional. Do **NOT** swap the polarity on the PWR_DUT power pins and GND; doing so can permanently damage the Gemini board.

3.1.3 DUT I/O Bank Power - V_{CCO}

The 400-pin DUT I/O test bus (200 pins per Xilinx Artix-7 FPGA) is directly connected to Artix FPGA I/O banks through the DUT Expansion Ports. Each bank consists of 50 DUT I/O pins, for a total of 8 banks, each of which are powered individually through their own V_{CCO} bank power rail. The DUT board must adequately budget power for each bank's V_{CCO} rails and provide the correct voltage/current needs depending on the specific I/O standard required for that respective bank's DUT I/O pins.

Important note: If the Gemini board is powered through the DC jack and the DUT board is powered through the PWR_DUT pins and the V_{CCO} rails are generated from PWR_DUT, make sure that power is not overdrawn from the PWR_DUT rail. This is dependent on the power supply chosen to power PWR_JACK and how much power it can supply. Please see the Recommended Operating Conditions section for power requirements.

Table 6 - DUT I/O Bank Voltage Rails (1)(2)

Artix Unit	Net Name	Description
Artix1	ARTIX1_VCCO_15	DUT I/O bank 15 rail
Artix1	ARTIX1_VCCO_16	DUT I/O bank 16 rail
Artix1	ARTIX1_VCCO_35	DUT I/O bank 35 rail
Artix1	ARTIX1_VCCO_36	DUT I/O bank 36 rail
Artix2	ARTIX2_VCCO_15	DUT I/O bank 15 rail
Artix2	ARTIX2_VCCO_34	DUT I/O bank 34 rail
Artix2	ARTIX2_VCCO_35	DUT I/O bank 35 rail
Artix2	ARTIX2_VCCO_36	DUT I/O bank 36 rail

Notes:

1. Please see the Xilinx Artix-7 DC and AC Switching Characteristics (DS181) document for more information on V_{CCO} bank and DUT I/O pin requirements and specifications.
2. Please see the Pin Definitions section to see how the DUT I/O pins are grouped into their respective V_{CCO} bank.

3.2 Power Sequencing

The Gemini board and the DUT board must be properly power sequenced to avoid damage to either board. The main Gemini board must be powered before the DUT board, regardless if its powered through the DC power jack or DUT Expansion Port power pins. The PWR_RESET_B (3.3V) signal will de-assert (go high) once power sequencing has completed. The DUT board is free to use this signal as a power good input to its own on-board power management system.

3.3 Status and Control Pins

Status, control and I²C signals are exposed to the DUT board through the DUT Expansion Port interface.

Note: If powering the Gemini board through the PWR_DUT rail, the DUT board must pull the PWR_ENABLE low until the PWR_DUT rail is stable. Once the Gemini board has finished power sequencing, it will pull PWR_RESET_B high, and the DUT board can continue its power sequence.

Important note: the Gemini board should not be randomly reset using either SOFT_RESET_B or PWR_ENABLE once PWR_ RESET_B de-asserts (goes high). The proper way to reset the board is by issuing a reset RPC call through the HTTP API or PyGemini API. Please see the Gemini User Guide for more information.

Table 7 – Status, Control and I²C Signals

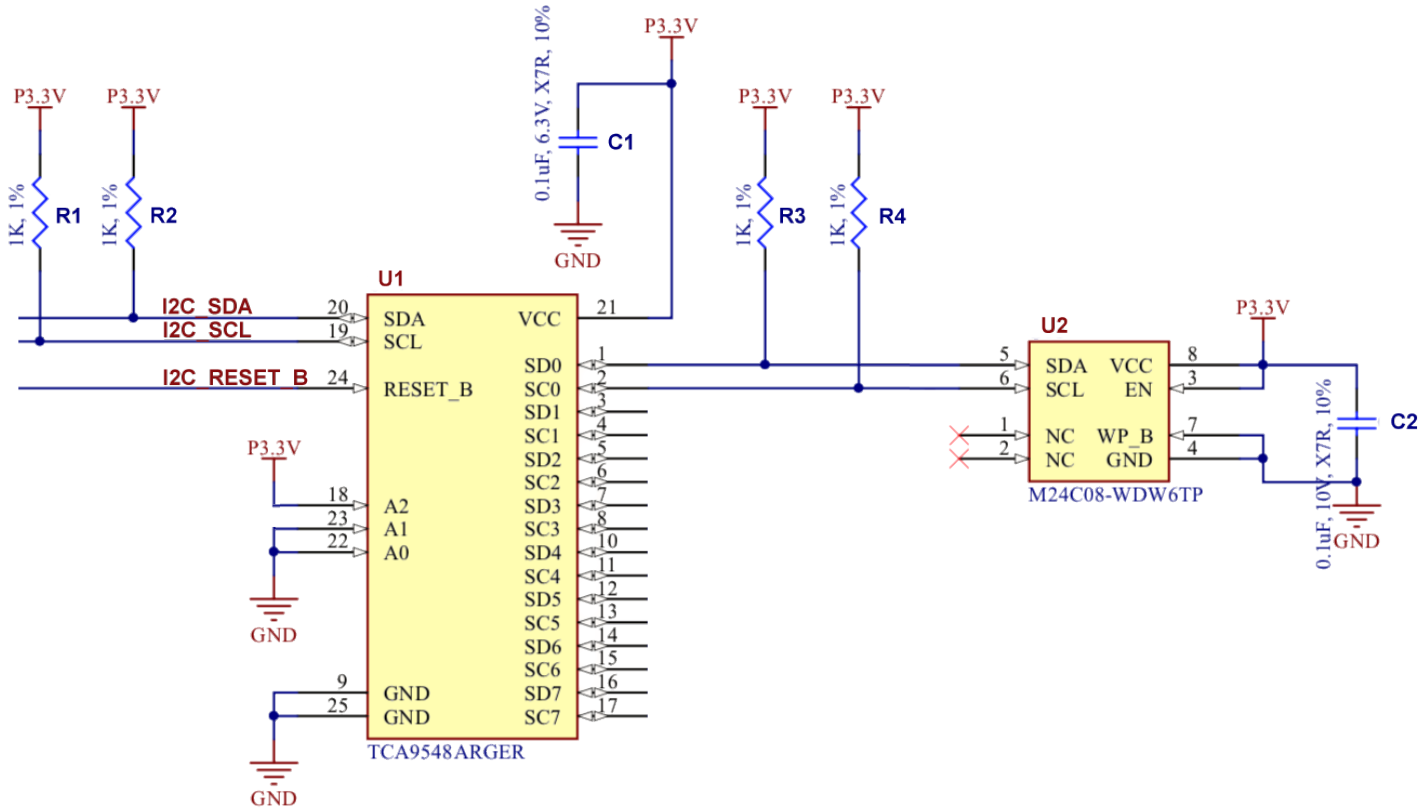
Name	Type	(V)	Description
PWR_RESET_B	O	3.3V	Push-pull CMOS signal. Driven high after power sequencing has completed, otherwise driven low.
SOFT_RESET_B	I	3.3V	Open-drain signal. Pulled high to 3.3V using 10k resistor. Pull signal low to soft reset the Gemini Board, otherwise let it float.
PWR_ENABLE	I	PWR_JACK or PWR_DUT	Open-drain signal. Pulled high to PWR_DUT using 10k resistor. Pull signal to low to hard reset the Gemini Board, otherwise let it float.
I2C_RESET_B	O	0V to 5V	Open-drain and not pulled up on the Gemini Board. It must be pulled up on the DUT board to a desired digital voltage level.
I2C_SCL	I/O	0V to 5V	Open-drain and not pulled up on the Gemini Board. It must be pulled up on the DUT board to a desired digital voltage level.
I2C_SDA	I/O	0V to 5V	Open-drain and not pulled up on the Gemini Board. It must be pulled up on the DUT board to a desired digital voltage level.

3.4 I²C Interface

All DUT boards are expected to have an EEPROM component connected to the I²C interface, preferably through an I²C switch. The purpose of the EEPROM component is to give VecOS™ a way to identify DUT boards and give it the ability to set and read DUT board configuration options, including capabilities, such as supported I/O standards. VecOS™ can check if a compiled test pattern binary stim file can run on a given DUT board and protect against invalid test-pattern stims running and damaging either the Gemini board or DUT board. Please see the Gemini User Guide for specifics of DUT board initialization.

Note: The size of the EEPROM must be at least 8Kb.

Figure 3 – I²C Switch and I²C EEPROM – Recommended Example Circuit



Note: the EEPROM component must be placed on channel 0 of the I²C switch

Table 8 – I²C Switch and I²C EEPROM - Component Recommendations (1)

Reference	Description	Part Number	Manufacturer
U1	IC I2C SW 8CH W/RESET 24VQFN	TCA9548ARGER	Texas Instruments
U2	IC EEPROM 8KBIT 400KHZ 8TSSOP	M24C08-WDW6TP	ST Microelectronics
C1, C2	CAP CER 0.1UF 10V X7R 20% 0603	CX0603MRX7R6BB104	Kemet
R1, R2, R3, R4	RES SMD 1K OHM 1% 1/10W 0603	RC0603FR-071KL	Yageo

Notes:

1. See *Third-Party Products* Disclaimer

Note: the I²C switch and EEPROM, in table 8, have been tested to work with the Gemini board. Using different components than recommended can lead to broken functionality.

3.5 Gigabit Ethernet

The Gigabit Ethernet controller supports 10Base-T, 100Base-TX and 1000Base-T speed modes and auto-negotiates upon peripheral insertion. The Gigabit Ethernet connector is a standard Ethernet receptacle with built-in magnetics and accepts standard CAT-5 unshielded twisted pair (UTP) cables.

3.6 USB 2.0

The on-board USB 2.0 controller operates only in host mode. When connected to a USB 2.0 peripheral, the controller operates in USB 2.0 High-Speed mode (480 MB/s). The controller will operate at USB 1.1 Full and Low Speed modes (12 MB/s) when connected to a USB 1.1 peripheral. The USB connector is a standard USB 2.0 Female Type-A connector.

3.7 SD Card

The SecureDigital (SD) controller is capable of interfacing directly to an external SD Card device. The controller is compatible with the standard *SD Host Controller Specification Version 2.0 Part A2* and can accept both SD high-speed (SDHS) and SD High Capacity (SDHC) card standards.

4 Physical / Electrical Characteristic

4.1 Absolute Maximum Ratings

The absolute maximum ratings must not be exceeded for any significant period of time. Operating at or beyond these parameters may damage and/or affect the long-term functionality of the Gemini board.

Table 9 - Power - Maximum Ratings

Symbol	Description	Min	Max	Unit
V_{PWR_JACK} (1)	Supply voltage from DC power jack	-0.3	20	V
V_{PWR_DUT} (1)	Supply voltage from DUT board PWR_DUT pins	-0.3	20	V
I_{PWR_JACK}	Current through power jack	–	5	A
I_{PWR_DUT}	Current through DUT board PWR_DUT pins	–	5	A

Notes:

1. V_{PWR_JACK} and V_{PWR_DUT} must not be powered at the same time.

Table 10 – DUT I/O – Maximum Ratings

V_{CCO} (1)	Supply voltage for DUT I/O banks	-0.5	3.6	V
$V_{DUT\_IO\_IN}$ (1)	DUT I/O input voltage	-0.4	V_{CCO} + 0.55	V

Notes:

1. Please see the Xilinx Artix-7 DC and AC Switching Characteristics (DS181) document for more information

Table 11 - PWR_RESET_B – Maximum Ratings

Symbol	Description		Min	Max	Unit
V_O(1)	Voltage range applied to any output in high-impedance or power-off state.		-0.5	6.5	V
V_O(1)	Voltage range applied to any output in the high or low state		-0.5	3.8	V
I_{OK}	Output clamp current	V_O < 0	–	-50	mA
I_O	Continuous output current		–	±50	mA

Notes:

1. The output negative-voltage ratings may be exceeded if the output current ratings are observed.

Table 12 – SOFT_RESET_B – Maximum Ratings

Symbol	Description		Min	Max	Unit
V_{IN}	DC Input Voltage		-0.5	7.0	V
I_{IN}	DC Input Diode Current	V_{IN} < -0.5 V	–	-50	mA

Table 13 - PWR_ENABLE – Maximum Ratings

Symbol	Description	Min	Max	Unit
V_{IN}	Input Voltage	-0.3	6.0	V
I_{IN}	Source Current	–	±100	µA

Table 14 - I2C_RESET_B - Maximum Ratings

Symbol	Description		Min	Max	Unit
V_{OUT}	DC Output Voltage		-0.5	7.0	V
I_{OK}	DC Output Diode Current	V_{OUT} < -0.5 V	–	-50	mA
I_{OUT}	DC Output Current		–	±50	mA

Table 15 - I2C_SCL, I2C_SDA – Maximum Ratings (1)(2)

Symbol	Description	Min	Max	Unit
V_I	Input Voltage	-0.5	7	V
I_I	Input Current	-20	20	mA
I_O	Output Current	-25	–	mA
I_{CC}	Supply Current	-100	100	mA

Notes:

1. I2C_SCL and I2C_SDA are connected to one lane of a TCA9548A I^2C switch, which uses a V_{CC} of 3.3v.
2. For more detailed information please see TCA9548A datasheet.

4.2 Recommended Operating Conditions

The parameters listed in the following tables specify the recommended operating ranges for the Gemini board.

Table 16 - Power – Recommended Conditions

Symbol	Description	Min	Nom	Max	Unit
V_{PWR_JACK}	Supply voltage from DC Jack	12	–	17	V
V_{PWR_DUT}	Supply voltage from PWR_DUT pins	12	–	17	V
I_{PWR_JACK}	Current through power jack	3	–	5	A
I_{PWR_DUT}	Current through DUT board PWR_DUT pins	3	–	5	A

Table 17 – DUT I/O – Recommended Conditions

V_{CCO} (1)	Supply voltage for DUT I/O banks	1.14	–	3.465	V
$V_{DUT\_IO\_IN}$ (1)	DUT I/O input voltage	-0.20	–	V_{CCO} + 0.20	V
$I_{DUT\_IO\_IN}$ (1)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode		–	10	mA

Notes:

1. Please see the Xilinx Artix-7 DC and AC Switching Characteristics (DS181) document for more information.

Table 18 - PWR_RESET_B – Recommended Conditions

Symbol	Description	Min	Nom	Max	Unit
V_O	Output Voltage	0	–	3.3	V
I_{OH}	High-level output current	–	–	-24	mA
I_{OL}	Low-level output current	–	–	24	mA

Table 19 – SOFT_RESET_B - Recommended Conditions

Symbol	Description	Min	Nom	Max	Unit
V_{IN}	Input Voltage	0	–	5.5	V
t_r, t_f	Input Rise and Fall Times	0	–	10	ns/V

Table 20 - I2C_RESET_B - Recommended Conditions

Symbol	Description	Min	Nom	Max	Unit
$V_{PULL-UP}$	Output Voltage (set with 1K pull-up on DUT board side)	0	–	5.5	V

Table 21 - I2C_SCL, I2C_SDA – Recommended Conditions (1)(2)

Symbol	Description	Min	Nom	Max	Unit
$V_{PULL-UP}$	Output Voltage (set with a pull-up (3) on DUT board side)	0	–	5.5	V

Notes:

1. I2C_SCL and I2C_SDA are connected to one lane of a TCA9548A I^2C switch, which uses a V_{CC} of 3.3v.
2. For more detailed information please see TCA9548A datasheet.
3. For choosing a pull-up resistor please see SLVA689 document.

4.3 Digital Logic

Any voltages less than the minimum value can be interpreted as a logic level low or as an undefined state, which may result in unreliable operation. Any voltage exceeding the maximum value can damage and adversely affect device reliability.

***Important note:* All DUT I/O V_{CCO} rails, corresponding to a Vector Engine, must be powered with the same voltage level and must use a matching I/O voltage standard as shown in table 22. The I/O voltage standard depends on the design requirements of the DUT board.**

Important note: selecting an I/O voltage standard that is incompatible with the attached DUT board can permanently damage the Gemini board and the DUT board.

Note: VecOS™ can dynamically switch the Vector Engine I/O standards through software depending on what is set in the configuration profile file. Please see the Gemini User Guide for more information.

Table 22 - DUT I/O - Input and Output Levels (1) (2)

I/O Standard	VCCO	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V Min	V Max	V Min	V Max	V Max	V Min	mA Max	mA Min
LVCMOS12	1.2	-0.300	35% VCCO	65% VCCO	VCCO + 0.300	0.400	VCCO - 0.400	8	8
LVCMOS15	1.5	-0.300	35% VCCO	65% VCCO	VCCO + 0.300	25% VCCO	75% VCCO	8	8
LVCMOS18	1.8	-0.300	35% VCCO	65% VCCO	VCCO + 0.300	0.450	VCCO - 0.450	8	8
LVCMOS25	2.5	-0.300	0.7	1.700	VCCO + 0.300	0.400	VCCO - 0.400	8	8
LVCMOS33	3.3	-0.300	0.8	2.000	3.450	0.400	VCCO - 0.400	8	8
LVTTL	3.3	-0.300	0.8	2.000	3.450	0.400	2.400	12	12

Notes:

1. For detailed interface specific DC voltage levels, see UG471: 7 Series FPGAs SelectIO Resources User Guide.
2. I/O Standards are set through the configuration *profile* file. Please see the Gemini User Guide for more information.

Table 23 – PWR_RESET_B – Output Levels

Symbol	Test Conditions	-40°C to 85°C			-40°C to 125°C RECOMMENDED			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{OH}	I_{OH} = -24 mA	2.3	-	-	2.3	-		V
V_{OL}	I_{OL} = 24 mA	-	-	0.55	-	-	0.55	V

Table 24 – SOFT_RESET_B – Input Level

Symbol	Description	T_A=+25° C			T_A=-40 to +85°C		Unit
		Min	Nom	Max	Min	Max	
V_{IH}	HIGH level input voltage	2.31	–	–	2.31	–	V
V_{IL}	LOW level input voltage	–	–	0.99	–	0.99	V
I_{IN}	Input Leakage Current	–	–	±0.1	–	±1.0	µA
I_{OFF}	Power Off Leakage Current	–	–	1	–	10	µA

Table 25 - I2C_RESET_B – Output Levels

Symbol	Description	Conditions	T_A=+25° C			T_A=-40 to +85°C		Unit
			Min	Nom	Max	Min	Max	
V_{OL}	LOW level output voltage	I_{OL}=100 µA	–	0.00	0.10	–	0.10	V
		I_{OL}=24 mA	–	0.24	0.55	–	0.55	V
I_{LKG}	HIGH Output Leakage Current	V_{OUT}=3.3 V or GND	–	–	±5	–	±10	µA

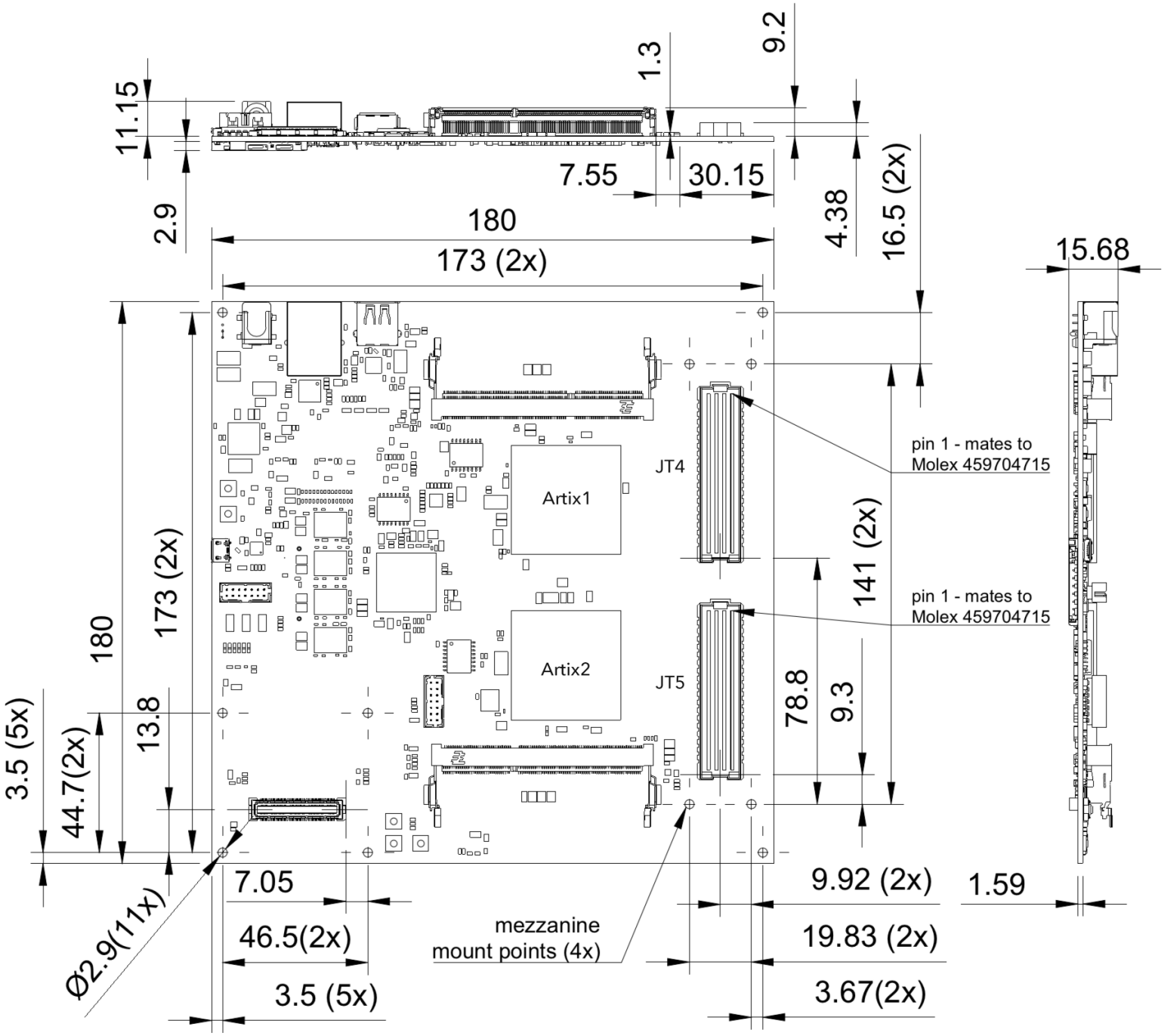
Table 26 - I2C_SCL, I2C_SDA – I/O Levels (1)(2)(3)

Symbol	Description	Conditions	Min	Nom	Max	Unit
I_{OL}	SDA	V_{OL} = 0.4 V	3	6	–	mA
		V_{OL} = 0.6 V	6	9	–	mA
$C_{IO(OFF)}$ (4)	SCL, SCD	Switch OFF	–	5.5	7.5	pF
V_{IH}	SCL, SDA		2.31	–	6	V
V_{IL}	SCL, SDA		-0.5	–	0.99	V

Notes:

1. I2C_SCL and I2C_SDA are connected to one lane of a TCA9548A I^2C switch, which uses a V_{CC} of 3.3v.
2. For more detailed information please see TCA9548A datasheet.
3. For choosing a pull-up resistor please see SLVA689 document.
4. $C_{IO(ON)}$ depends on internal capacitance and external capacitance added to the SCL line when channel is ON.

4.4 Board Drawings and Dimensions



Note: all units are in mm unless otherwise noted

Note: when designing the DUT board, care must be taken so that the card does not overextend into the other components on the Gemini board

4.5 DUT Expansion Ports – Molex Connectors

The Gemini board uses two high-density, 400-pin Molex female connectors to do a board-to-board connection to the DUT board. The DUT board must use the corresponding compatible Molex male connector shown in table 28 below.

Note: please check that the total mating height of the Gemini board with the DUT board does not exceed your design requirements.

Note: please refer to Molex documentation on the proper mating procedure. Improper mating can lead to damaged boards and/or connectors.

Table 27 – Gemini Board Molex Female Connectors

Reference	Description	Part Number	Manufacturer
JT4, JT5	10-row 400-position vertical SMD gold receptacle	45971-4115	Molex

Table 28 – DUT board Molex Male Connectors (1)

Description	Part Number	Manufacturer
10-row 400-pos vertical SMD gold plug	45970-4715	Molex

Notes:

1. See *Third-Party Products* Disclaimer

4.6 High-Speed Expansion Port

The high-speed expansion port is currently reserved for future use.

5 Pin Definitions

Note: All GND pins must be connected to ground and not left floating.

Note: All RSVD pins must **NOT** be connected to ground and must be left floating.

Note: All single-ended interface ports are routed with a controlled impedance of 50 Ω ± 5 Ω except for pins with a *Pin Type* of *GND* or *Power In*

Table 29 – DUT Expansion Port Interface

Artix Unit	Molex Unit	Molex Pin	V_{CCO} Bank	Pin Name	Description	Direction	Pin Type
1	JT4	1	–	GND	GND	–	GND
1	JT4	2	–	GND	GND	–	GND
1	JT4	3	–	GND	GND	–	GND
1	JT4	4	35	ARTIX1_DUT_IO_0	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	5	–	GND	GND	–	GND
1	JT4	6	35	ARTIX1_DUT_IO_2	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	7	–	GND	GND	–	GND
1	JT4	8	35	ARTIX1_DUT_IO_4	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	9	–	GND	GND	–	GND
1	JT4	10	35	ARTIX1_DUT_IO_6	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	11	–	GND	GND	–	GND

1	JT4	12	36	ARTIX1_DUT_IO_8	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	13	–	GND	GND	–	GND
1	JT4	14	35	ARTIX1_DUT_IO_50	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	15	–	GND	GND	–	GND
1	JT4	16	35	ARTIX1_DUT_IO_52	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	17	–	GND	GND	–	GND
1	JT4	18	35	ARTIX1_DUT_IO_54	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	19	–	GND	GND	–	GND
1	JT4	20	35	ARTIX1_DUT_IO_56	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	21	–	GND	GND	–	GND
1	JT4	22	35	ARTIX1_DUT_IO_58	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	23	–	GND	GND	–	GND
1	JT4	24	–	GND	GND	–	GND
1	JT4	25	16	ARTIX1_DUT_IO_100	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	26	16	ARTIX1_DUT_IO_102	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	27	16	ARTIX1_DUT_IO_104	DUT I/O	Bidir	CMOS/TTL - I/O Standard

1	JT4	28	16	ARTIX1_DUT_IO_106	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	29	16	ARTIX1_DUT_IO_108	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	30	16	ARTIX1_DUT_IO_110	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	31	16	ARTIX1_DUT_IO_112	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	32	–	GND	GND	–	GND
1	JT4	33	16	ARTIX1_DUT_IO_150	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	34	16	ARTIX1_DUT_IO_152	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	35	16	ARTIX1_DUT_IO_154	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	36	16	ARTIX1_DUT_IO_156	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	37	15	ARTIX1_DUT_IO_158	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	38	16	ARTIX1_DUT_IO_160	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	39	16	ARTIX1_DUT_IO_162	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	40	–	GND	GND	–	GND

1	JT4	41	–	GND	GND	–	GND
1	JT4	42	–	GND	GND	–	GND
1	JT4	43	–	GND	GND	–	GND
1	JT4	44	–	GND	GND	–	GND
1	JT4	45	35	ARTIX1_DUT_IO_1	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	46	–	GND	GND	–	GND
1	JT4	47	35	ARTIX1_DUT_IO_3	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	48	–	GND	GND	–	GND
1	JT4	49	35	ARTIX1_DUT_IO_5	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	50	–	GND	GND	–	GND
1	JT4	51	36	ARTIX1_DUT_IO_7	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	52	–	GND	GND	–	GND
1	JT4	53	36	ARTIX1_DUT_IO_9	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	54	–	GND	GND	–	GND
1	JT4	55	35	ARTIX1_DUT_IO_51	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	56	–	GND	GND	–	GND
1	JT4	57	35	ARTIX1_DUT_IO_53	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	58	–	GND	GND	–	GND

1	JT4	59	35	ARTIX1_DUT_IO_55	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	60	–	GND	GND	–	GND
1	JT4	61	35	ARTIX1_DUT_IO_57	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	62	–	GND	GND	–	GND
1	JT4	63	35	ARTIX1_DUT_IO_59	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	64	–	GND	GND	–	GND
1	JT4	65	16	ARTIX1_DUT_IO_101	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	66	16	ARTIX1_DUT_IO_103	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	67	16	ARTIX1_DUT_IO_105	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	68	16	ARTIX1_DUT_IO_107	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	69	16	ARTIX1_DUT_IO_109	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	70	16	ARTIX1_DUT_IO_111	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	71	16	ARTIX1_DUT_IO_113	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	72	–	GND	GND	–	GND

1	JT4	73	16	ARTIX1_DUT_IO_151	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	74	16	ARTIX1_DUT_IO_153	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	75	16	ARTIX1_DUT_IO_155	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	76	15	ARTIX1_DUT_IO_157	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	77	15	ARTIX1_DUT_IO_159	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	78	15	ARTIX1_DUT_IO_161	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	79	16	ARTIX1_DUT_IO_163	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	80	–	GND	GND	–	GND
1	JT4	81	–	GND	GND	–	GND
1	JT4	82	35	ARTIX1_DUT_IO_30	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	83	–	GND	GND	–	GND
1	JT4	84	35	ARTIX1_DUT_IO_10	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	85	–	GND	GND	–	GND
1	JT4	86	35	ARTIX1_DUT_IO_12	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	87	–	GND	GND	–	GND

1	JT4	88	36	ARTIX1_DUT_IO_14	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	89	–	GND	GND	–	GND
1	JT4	90	36	ARTIX1_DUT_IO_16	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	91	–	GND	GND	–	GND
1	JT4	92	36	ARTIX1_DUT_IO_18	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	93	–	GND	GND	–	GND
1	JT4	94	35	ARTIX1_DUT_IO_60	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	95	–	GND	GND	–	GND
1	JT4	96	35	ARTIX1_DUT_IO_62	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	97	–	GND	GND	–	GND
1	JT4	98	35	ARTIX1_DUT_IO_64	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	99	–	GND	GND	–	GND
1	JT4	100	35	ARTIX1_DUT_IO_66	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	101	–	GND	GND	–	GND
1	JT4	102	35	ARTIX1_DUT_IO_68	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	103	–	GND	GND	–	GND
1	JT4	104	–	GND	GND	–	GND

1	JT4	105	16	ARTIX1_DUT_IO_114	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	106	16	ARTIX1_DUT_IO_116	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	107	16	ARTIX1_DUT_IO_118	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	108	15	ARTIX1_DUT_IO_120	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	109	16	ARTIX1_DUT_IO_122	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	110	15	ARTIX1_DUT_IO_124	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	111	15	ARTIX1_DUT_IO_126	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	112	–	GND	GND	–	GND
1	JT4	113	15	ARTIX1_DUT_IO_164	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	114	15	ARTIX1_DUT_IO_166	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	115	15	ARTIX1_DUT_IO_168	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	116	16	ARTIX1_DUT_IO_170	DUT I/O	Bidir	CMOS/TTL - I/O Standard

1	JT4	117	15	ARTIX1_DUT_IO_172	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	118	15	ARTIX1_DUT_IO_174	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	119	15	ARTIX1_DUT_IO_176	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	120	–	GND	GND	–	GND
1	JT4	121	35	ARTIX1_DUT_IO_20	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	122	–	GND	GND	–	GND
1	JT4	123	35	ARTIX1_DUT_IO_21	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	124	–	GND	GND	–	GND
1	JT4	125	35	ARTIX1_DUT_IO_11	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	126	–	GND	GND	–	GND
1	JT4	127	35	ARTIX1_DUT_IO_13	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	128	–	GND	GND	–	GND
1	JT4	129	36	ARTIX1_DUT_IO_15	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	130	–	GND	GND	–	GND
1	JT4	131	36	ARTIX1_DUT_IO_17	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	132	–	GND	GND	–	GND

1	JT4	133	36	ARTIX1_DUT_IO_19	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	134	–	GND	GND	–	GND
1	JT4	135	35	ARTIX1_DUT_IO_61	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	136	–	GND	GND	–	GND
1	JT4	137	35	ARTIX1_DUT_IO_63	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	138	–	GND	GND	–	GND
1	JT4	139	35	ARTIX1_DUT_IO_65	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	140	–	GND	GND	–	GND
1	JT4	141	35	ARTIX1_DUT_IO_67	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	142	–	GND	GND	–	GND
1	JT4	143	35	ARTIX1_DUT_IO_69	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	144	–	GND	GND	–	GND
1	JT4	145	16	ARTIX1_DUT_IO_115	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	146	16	ARTIX1_DUT_IO_117	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	147	16	ARTIX1_DUT_IO_119	DUT I/O	Bidir	CMOS/TTL - I/O Standard

1	JT4	148	16	ARTIX1_DUT_IO_121	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	149	15	ARTIX1_DUT_IO_123	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	150	16	ARTIX1_DUT_IO_125	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	151	16	ARTIX1_DUT_IO_127	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	152	–	GND	GND	–	GND
1	JT4	153	15	ARTIX1_DUT_IO_165	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	154	15	ARTIX1_DUT_IO_167	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	155	16	ARTIX1_DUT_IO_169	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	156	16	ARTIX1_DUT_IO_171	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	157	15	ARTIX1_DUT_IO_173	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	158	15	ARTIX1_DUT_IO_175	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	159	15	ARTIX1_DUT_IO_177	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	160	–	GND	GND	–	GND

1	JT4	161	–	GND	GND	–	GND
1	JT4	162	–	GND	GND	–	GND
1	JT4	163	–	GND	GND	–	GND
1	JT4	164	35	ARTIX1_DUT_IO_22	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	165	–	GND	GND	–	GND
1	JT4	166	35	ARTIX1_DUT_IO_24	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	167	–	GND	GND	–	GND
1	JT4	168	35	ARTIX1_DUT_IO_26	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	169	–	GND	GND	–	GND
1	JT4	170	35	ARTIX1_DUT_IO_28	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	171	–	GND	GND	–	GND
1	JT4	172	36	ARTIX1_DUT_IO_70	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	173	–	GND	GND	–	GND
1	JT4	174	35	ARTIX1_DUT_IO_72	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	175	–	GND	GND	–	GND
1	JT4	176	35	ARTIX1_DUT_IO_74	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	177	–	GND	GND	–	GND

1	JT4	178	35	ARTIX1_DUT_IO_76	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	179	–	GND	GND	–	GND
1	JT4	180	35	ARTIX1_DUT_IO_78	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	181	–	GND	GND	–	GND
1	JT4	182	–	GND	GND	–	GND
1	JT4	183	35	ARTIX1_DUT_IO_128	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	184	16	ARTIX1_DUT_IO_130	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	185	16	ARTIX1_DUT_IO_132	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	186	16	ARTIX1_DUT_IO_134	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	187	15	ARTIX1_DUT_IO_136	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	188	15	ARTIX1_DUT_IO_138	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	189	16	ARTIX1_DUT_IO_140	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	190	–	GND	GND	–	GND
1	JT4	191	15	ARTIX1_DUT_IO_178	DUT I/O	Bidir	CMOS/TTL - I/O Standard

1	JT4	192	16	ARTIX1_DUT_IO_180	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	193	15	ARTIX1_DUT_IO_182	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	194	15	ARTIX1_DUT_IO_184	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	195	16	ARTIX1_DUT_IO_186	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	196	16	ARTIX1_DUT_IO_188	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	197	15	ARTIX1_DUT_IO_190	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	198	–	GND	GND	–	GND
1	JT4	199	–	GND	GND	–	GND
1	JT4	200	–	GND	GND	–	GND
1	JT4	201	–	GND	GND	–	GND
1	JT4	202	–	GND	GND	–	GND
1	JT4	203	35	ARTIX1_DUT_IO_31	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	204	–	GND	GND	–	GND
1	JT4	205	35	ARTIX1_DUT_IO_23	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	206	–	GND	GND	–	GND
1	JT4	207	36	ARTIX1_DUT_IO_25	DUT I/O	Bidir	CMOS/TTL - I/O Standard

1	JT4	208	–	GND	GND	–	GND
1	JT4	209	36	ARTIX1_DUT_IO_27	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	210	–	GND	GND	–	GND
1	JT4	211	36	ARTIX1_DUT_IO_29	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	212	–	GND	GND	–	GND
1	JT4	213	36	ARTIX1_DUT_IO_71	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	214	–	GND	GND	–	GND
1	JT4	215	36	ARTIX1_DUT_IO_73	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	216	–	GND	GND	–	GND
1	JT4	217	36	ARTIX1_DUT_IO_75	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	218	–	GND	GND	–	GND
1	JT4	219	36	ARTIX1_DUT_IO_77	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	220	–	GND	GND	–	GND
1	JT4	221	36	ARTIX1_DUT_IO_79	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	222	–	GND	GND	–	GND
1	JT4	223	16	ARTIX1_DUT_IO_129	DUT I/O	Bidir	CMOS/TTL - I/O Standard

1	JT4	224	15	ARTIX1_DUT_IO_131	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	225	15	ARTIX1_DUT_IO_133	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	226	15	ARTIX1_DUT_IO_135	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	227	15	ARTIX1_DUT_IO_137	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	228	15	ARTIX1_DUT_IO_139	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	229	15	ARTIX1_DUT_IO_141	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	230	–	GND	GND	–	GND
1	JT4	231	15	ARTIX1_DUT_IO_179	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	232	15	ARTIX1_DUT_IO_181	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	233	15	ARTIX1_DUT_IO_183	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	234	15	ARTIX1_DUT_IO_185	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	235	15	ARTIX1_DUT_IO_187	DUT I/O	Bidir	CMOS/TTL - I/O Standard

1	JT4	236	15	ARTIX1_DUT_IO_189	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	237	15	ARTIX1_DUT_IO_191	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	238	–	GND	GND	–	GND
1	JT4	239	–	GND	GND	–	GND
1	JT4	240	–	GND	GND	–	GND
1	JT4	241	35	ARTIX1_VCCO_35	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	242	35	ARTIX1_VCCO_35	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	243	–	GND	GND	–	GND
1	JT4	244	35	ARTIX1_DUT_IO_32	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	245	–	GND	GND	–	GND
1	JT4	246	36	ARTIX1_DUT_IO_34	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	247	–	GND	GND	–	GND
1	JT4	248	36	ARTIX1_DUT_IO_36	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	249	–	GND	GND	–	GND
1	JT4	250	36	ARTIX1_DUT_IO_38	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	251	–	GND	GND	–	GND

1	JT4	252	36	ARTIX1_DUT_IO_80	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	253	–	GND	GND	–	GND
1	JT4	254	36	ARTIX1_DUT_IO_82	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	255	–	GND	GND	–	GND
1	JT4	256	36	ARTIX1_DUT_IO_84	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	257	–	GND	GND	–	GND
1	JT4	258	36	ARTIX1_DUT_IO_86	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	259	–	GND	GND	–	GND
1	JT4	260	36	ARTIX1_DUT_IO_88	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	261	–	GND	GND	–	GND
1	JT4	262	–	GND	GND	–	GND
1	JT4	263	16	ARTIX1_DUT_IO_142	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	264	–	GND	GND	–	GND
1	JT4	265	15	ARTIX1_DUT_IO_144	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	266	–	GND	GND	–	GND
1	JT4	267	16	ARTIX1_DUT_IO_146	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	268	–	GND	GND	–	GND

1	JT4	269	15	ARTIX1_DUT_IO_148	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	270	–	GND	GND	–	GND
1	JT4	271	15	ARTIX1_DUT_IO_192	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	272	–	GND	GND	–	GND
1	JT4	273	15	ARTIX1_DUT_IO_194	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	274	–	GND	GND	–	GND
1	JT4	275	15	ARTIX1_DUT_IO_196	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	276	–	GND	GND	–	GND
1	JT4	277	15	ARTIX1_DUT_IO_198	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	278	–	GND	GND	–	GND
1	JT4	279	15	ARTIX1_VCCO_15	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	280	15	ARTIX1_VCCO_15	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	281	35	ARTIX1_VCCO_35	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	282	35	ARTIX1_VCCO_35	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	283	–	GND	GND	–	GND
1	JT4	284	–	GND	GND	–	GND

1	JT4	285	35	ARTIX1_DUT_IO_33	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	286	–	GND	GND	–	GND
1	JT4	287	35	ARTIX1_DUT_IO_35	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	288	–	GND	GND	–	GND
1	JT4	289	36	ARTIX1_DUT_IO_37	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	290	–	GND	GND	–	GND
1	JT4	291	36	ARTIX1_DUT_IO_39	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	292	–	GND	GND	–	GND
1	JT4	293	36	ARTIX1_DUT_IO_81	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	294	–	GND	GND	–	GND
1	JT4	295	36	ARTIX1_DUT_IO_83	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	296	–	GND	GND	–	GND
1	JT4	297	36	ARTIX1_DUT_IO_85	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	298	–	GND	GND	–	GND
1	JT4	299	36	ARTIX1_DUT_IO_87	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	300	–	GND	GND	–	GND

1	JT4	301	36	ARTIX1_DUT_IO_89	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	302	–	GND	GND	–	GND
1	JT4	303	16	ARTIX1_DUT_IO_143	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	304	–	GND	GND	–	GND
1	JT4	305	15	ARTIX1_DUT_IO_145	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	306	–	GND	GND	–	GND
1	JT4	307	16	ARTIX1_DUT_IO_147	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	308	–	GND	GND	–	GND
1	JT4	309	15	ARTIX1_DUT_IO_149	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	310	–	GND	GND	–	GND
1	JT4	311	15	ARTIX1_DUT_IO_193	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	312	–	GND	GND	–	GND
1	JT4	313	15	ARTIX1_DUT_IO_195	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	314	–	GND	GND	–	GND
1	JT4	315	15	ARTIX1_DUT_IO_197	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	316	–	GND	GND	–	GND

1	JT4	317	15	ARTIX1_DUT_IO_199	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	318	–	GND	GND	–	GND
1	JT4	319	15	ARTIX1_VCCO_15	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	320	15	ARTIX1_VCCO_15	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	321	36	ARTIX1_VCCO_36	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	322	36	ARTIX1_VCCO_36	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	323	–	GND	GND	–	GND
1	JT4	324	35	ARTIX1_DUT_IO_90	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	325	–	GND	GND	–	GND
1	JT4	326	36	ARTIX1_DUT_IO_92	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	327	–	GND	GND	–	GND
1	JT4	328	36	ARTIX1_DUT_IO_94	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	329	–	GND	GND	–	GND
1	JT4	330	36	ARTIX1_DUT_IO_96	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	331	–	GND	GND	–	GND

1	JT4	332	36	ARTIX1_DUT_IO_98	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	333	–	GND	GND	–	GND
1	JT4	334	36	ARTIX1_DUT_IO_40	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	335	–	GND	GND	–	GND
1	JT4	336	36	ARTIX1_DUT_IO_42	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	337	–	GND	GND	–	GND
1	JT4	338	36	ARTIX1_DUT_IO_44	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	339	–	GND	GND	–	GND
1	JT4	340	36	ARTIX1_DUT_IO_46	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	341	–	GND	GND	–	GND
1	JT4	342	35	ARTIX1_DUT_IO_48	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	343	–	GND	GND	–	GND
1	JT4	344	–	I2C_SCL	I^2C Clock	Bidir	Open-drain - not pulled up on Gemini board. Pull up to desired voltage level.
1	JT4	345	–	I2C_RESET_B	I^2C Reset	Output	Open-drain - not pulled

							up on Gemini board. Pull up to desired voltage level.
1	JT4	346	–	I2C_SDA	I^2C Data	Bidir	Open-drain - not pulled up on Gemini board. Pull up to desired voltage level.
1	JT4	347	–	GND	GND	–	GND
1	JT4	348	–	GND	GND	–	GND
1	JT4	349	–	GND	GND	–	GND
1	JT4	350	–	GND	GND	–	GND
1	JT4	351	–	GND	GND	–	GND
1	JT4	352	–	GND	GND	–	GND
1	JT4	353	–	GND	GND	–	GND
1	JT4	354	–	GND	GND	–	GND
1	JT4	355	–	GND	GND	–	GND
1	JT4	356	–	GND	GND	–	GND
1	JT4	357	–	GND	GND	–	GND
1	JT4	358	–	GND	GND	–	GND
1	JT4	359	16	ARTIX1_VCCO_16	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	360	16	ARTIX1_VCCO_16	DUT I/O VCCO Power	Input	Power In - I/O Standard

1	JT4	361	36	ARTIX1_VCCO_36	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	362	36	ARTIX1_VCCO_36	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	363	–	GND	GND	–	GND
1	JT4	364	–	GND	GND	–	GND
1	JT4	365	36	ARTIX1_DUT_IO_91	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	366	–	GND	GND	–	GND
1	JT4	367	36	ARTIX1_DUT_IO_93	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	368	–	GND	GND	–	GND
1	JT4	369	36	ARTIX1_DUT_IO_95	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	370	–	GND	GND	–	GND
1	JT4	371	36	ARTIX1_DUT_IO_97	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	372	–	GND	GND	–	GND
1	JT4	373	36	ARTIX1_DUT_IO_99	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	374	–	GND	GND	–	GND
1	JT4	375	36	ARTIX1_DUT_IO_41	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	376	–	GND	GND	–	GND

1	JT4	377	36	ARTIX1_DUT_IO_43	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	378	–	GND	GND	–	GND
1	JT4	379	36	ARTIX1_DUT_IO_45	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	380	–	GND	GND	–	GND
1	JT4	381	36	ARTIX1_DUT_IO_47	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	382	–	GND	GND	–	GND
1	JT4	383	16	ARTIX1_DUT_IO_49	DUT I/O	Bidir	CMOS/TTL - I/O Standard
1	JT4	384	–	GND	GND	–	GND
1	JT4	385	–	GND	GND	–	GND
1	JT4	386	–	GND	GND	–	GND
1	JT4	387	–	GND	GND	–	GND
1	JT4	388	–	GND	GND	–	GND
1	JT4	389	–	GND	GND	–	GND
1	JT4	390	–	GND	GND	–	GND
1	JT4	391	–	GND	GND	–	GND
1	JT4	392	–	GND	GND	–	GND
1	JT4	393	–	GND	GND	–	GND
1	JT4	394	–	GND	GND	–	GND
1	JT4	395	–	GND	GND	–	GND
1	JT4	396	–	RSVD	No Connect	–	–
1	JT4	397	–	RSVD	No Connect	–	–
1	JT4	398	–	GND	GND	–	GND

1	JT4	399	16	ARTIX1_VCCO_16	DUT I/O VCCO Power	Input	Power In - I/O Standard
1	JT4	400	16	ARTIX1_VCCO_16	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	1	–	RSVD	No connect	–	–
2	JT5	2	–	GND	GND	–	GND
2	JT5	3	–	RSVD	No connect	–	–
2	JT5	4	–	RSVD	No connect	–	–
2	JT5	5	–	GND	GND	–	GND
2	JT5	6	–	RSVD	No connect	–	–
2	JT5	7	–	RSVD	No connect	–	–
2	JT5	8	–	RSVD	No connect	–	–
2	JT5	9	–	RSVD	No connect	–	–
2	JT5	10	–	GND	GND	–	GND
2	JT5	11	36	ARTIX2_DUT_IO_0	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	12	36	ARTIX2_DUT_IO_1	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	13	36	ARTIX2_DUT_IO_2	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	14	36	ARTIX2_DUT_IO_3	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	15	36	ARTIX2_DUT_IO_4	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	16	36	ARTIX2_DUT_IO_50	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	17	36	ARTIX2_DUT_IO_51	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	18	36	ARTIX2_DUT_IO_52	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	19	36	ARTIX2_DUT_IO_53	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	20	35	ARTIX2_DUT_IO_54	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	21	–	GND	GND	–	GND
2	JT5	22	15	ARTIX2_DUT_IO_100	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	23	15	ARTIX2_DUT_IO_101	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	24	15	ARTIX2_DUT_IO_102	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	25	15	ARTIX2_DUT_IO_103	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	26	15	ARTIX2_DUT_IO_104	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	27	–	GND	GND	–	GND
2	JT5	28	15	ARTIX2_DUT_IO_150	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	29	15	ARTIX2_DUT_IO_151	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	30	15	ARTIX2_DUT_IO_152	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	31	15	ARTIX2_DUT_IO_153	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	32	15	ARTIX2_DUT_IO_154	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	33	–	GND	GND	–	GND
2	JT5	34	–	RSVD	No Connect	–	–
2	JT5	35	–	RSVD	No Connect	–	–
2	JT5	36	–	RSVD	No Connect	–	–
2	JT5	37	–	RSVD	No Connect	–	–
2	JT5	38	–	RSVD	No Connect	–	–
2	JT5	39	–	RSVD	No connect	–	–
2	JT5	40	–	RSVD	No connect	–	–
2	JT5	41	–	RSVD	No Connect	–	–
2	JT5	42	–	GND	GND	–	GND
2	JT5	43	–	GND	GND	–	GND
2	JT5	44	–	GND	GND	–	GND
2	JT5	45	–	GND	GND	–	GND
2	JT5	46	–	GND	GND	–	GND
2	JT5	47	–	GND	GND	–	GND
2	JT5	48	–	GND	GND	–	GND
2	JT5	49	–	GND	GND	–	GND

2	JT5	50	36	ARTIX2_DUT_IO_5	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	51	36	ARTIX2_DUT_IO_6	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	52	36	ARTIX2_DUT_IO_7	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	53	36	ARTIX2_DUT_IO_8	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	54	36	ARTIX2_DUT_IO_9	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	55	–	GND	GND	–	GND
2	JT5	56	36	ARTIX2_DUT_IO_55	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	57	36	ARTIX2_DUT_IO_56	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	58	36	ARTIX2_DUT_IO_57	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	59	36	ARTIX2_DUT_IO_58	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	60	15	ARTIX2_DUT_IO_59	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	61	–	GND	GND	–	GND
2	JT5	62	15	ARTIX2_DUT_IO_105	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	63	15	ARTIX2_DUT_IO_106	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	64	15	ARTIX2_DUT_IO_107	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	65	15	ARTIX2_DUT_IO_108	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	66	15	ARTIX2_DUT_IO_109	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	67	–	GND	GND	–	GND
2	JT5	68	15	ARTIX2_DUT_IO_155	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	69	15	ARTIX2_DUT_IO_156	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	70	15	ARTIX2_DUT_IO_157	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	71	15	ARTIX2_DUT_IO_158	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	72	15	ARTIX2_DUT_IO_159	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	73	–	GND	GND	–	GND
2	JT5	74	–	RSVD	No Connect	–	–
2	JT5	75	–	RSVD	No Connect	–	–
2	JT5	76	–	RSVD	No Connect	–	–
2	JT5	77	–	RSVD	No connect	–	–

2	JT5	78	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	79	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	80	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	81	–	GND	GND	–	GND
2	JT5	82	35	ARTIX2_DUT_IO_194	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	83	35	ARTIX2_DUT_IO_199	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	84	36	ARTIX2_DUT_IO_184	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	85	35	ARTIX2_DUT_IO_189	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	86	–	GND	GND	–	GND
2	JT5	87	–	RSVD	No Connect	–	–
2	JT5	88	–	RSVD	No connect	–	–
2	JT5	89	–	GND	GND	–	GND
2	JT5	90	36	ARTIX2_DUT_IO_10	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	91	36	ARTIX2_DUT_IO_11	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	92	36	ARTIX2_DUT_IO_12	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	93	36	ARTIX2_DUT_IO_13	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	94	36	ARTIX2_DUT_IO_14	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	95	–	GND	GND	–	GND
2	JT5	96	36	ARTIX2_DUT_IO_60	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	97	36	ARTIX2_DUT_IO_61	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	98	36	ARTIX2_DUT_IO_62	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	99	36	ARTIX2_DUT_IO_63	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	100	36	ARTIX2_DUT_IO_64	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	101	–	GND	GND	–	GND
2	JT5	102	15	ARTIX2_DUT_IO_110	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	103	15	ARTIX2_DUT_IO_111	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	104	15	ARTIX2_DUT_IO_112	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	105	15	ARTIX2_DUT_IO_113	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	106	15	ARTIX2_DUT_IO_114	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	107	–	GND	GND	–	GND
2	JT5	108	15	ARTIX2_DUT_IO_160	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	109	15	ARTIX2_DUT_IO_161	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	110	15	ARTIX2_DUT_IO_162	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	111	15	ARTIX2_DUT_IO_163	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	112	15	ARTIX2_DUT_IO_164	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	113	–	GND	GND	–	GND
2	JT5	114	–	RSVD	No connect	–	–
2	JT5	115	36	ARTIX2_VCCO_36	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	116	36	ARTIX2_VCCO_36	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	117	–	RSVD	No connect	–	–
2	JT5	118	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	119	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	120	–	PWR_DUT	DUT board power input	Input	12V-17V

2	JT5	121	–	RSVD	No connect	–	–
2	JT5	122	–	GND	GND	–	GND
2	JT5	123	35	ARTIX2_DUT_IO_193	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	124	36	ARTIX2_DUT_IO_198	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	125	35	ARTIX2_DUT_IO_183	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	126	35	ARTIX2_DUT_IO_188	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	127	–	GND	GND	–	GND
2	JT5	128	–	GND	GND	–	GND
2	JT5	129	–	GND	GND	–	GND
2	JT5	130	36	ARTIX2_DUT_IO_15	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	131	34	ARTIX2_DUT_IO_16	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	132	35	ARTIX2_DUT_IO_17	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	133	35	ARTIX2_DUT_IO_18	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	134	34	ARTIX2_DUT_IO_19	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	135	–	GND	GND	–	GND

2	JT5	136	36	ARTIX2_DUT_IO_65	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	137	36	ARTIX2_DUT_IO_66	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	138	35	ARTIX2_DUT_IO_67	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	139	36	ARTIX2_DUT_IO_68	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	140	36	ARTIX2_DUT_IO_69	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	141	–	GND	GND	–	GND
2	JT5	142	36	ARTIX2_DUT_IO_115	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	143	34	ARTIX2_DUT_IO_116	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	144	15	ARTIX2_DUT_IO_117	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	145	15	ARTIX2_DUT_IO_118	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	146	15	ARTIX2_DUT_IO_119	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	147	–	GND	GND	–	GND
2	JT5	148	15	ARTIX2_DUT_IO_165	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	149	15	ARTIX2_DUT_IO_166	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	150	15	ARTIX2_DUT_IO_167	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	151	15	ARTIX2_DUT_IO_168	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	152	–	RSVD	No connect	–	–
2	JT5	153	–	GND	GND	–	GND
2	JT5	154	–	RSVD	No connect	–	–
2	JT5	155	36	ARTIX2_VCCO_36	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	156	36	ARTIX2_VCCO_36	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	157	–	RSVD	No connect	–	–
2	JT5	158	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	159	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	160	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	161	–	RSVD	No connect	–	–
2	JT5	162	–	RSVD	No connect	–	–
2	JT5	163	35	ARTIX2_DUT_IO_192	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	164	36	ARTIX2_DUT_IO_197	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	165	36	ARTIX2_DUT_IO_182	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	166	35	ARTIX2_DUT_IO_187	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	167	–	RSVD	No connect	–	–
2	JT5	168	–	SOFT_RESET_B	Soft reset	Input	Open-drain - pulled to 3.3V using 10k resistor
2	JT5	169	–	GND	GND	–	GND
2	JT5	170	36	ARTIX2_DUT_IO_20	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	171	35	ARTIX2_DUT_IO_21	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	172	36	ARTIX2_DUT_IO_22	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	173	35	ARTIX2_DUT_IO_23	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	174	34	ARTIX2_DUT_IO_24	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	175	–	GND	GND	–	GND
2	JT5	176	34	ARTIX2_DUT_IO_70	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	177	35	ARTIX2_DUT_IO_71	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	178	36	ARTIX2_DUT_IO_72	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	179	35	ARTIX2_DUT_IO_73	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	180	35	ARTIX2_DUT_IO_74	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	181	–	GND	GND	–	GND
2	JT5	182	35	ARTIX2_DUT_IO_120	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	183	34	ARTIX2_DUT_IO_121	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	184	15	ARTIX2_DUT_IO_122	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	185	15	ARTIX2_DUT_IO_123	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	186	15	ARTIX2_DUT_IO_124	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	187	–	GND	GND	–	GND
2	JT5	188	15	ARTIX2_DUT_IO_170	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	189	15	ARTIX2_DUT_IO_171	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	190	15	ARTIX2_DUT_IO_172	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	191	–	GND	GND	–	GND
2	JT5	192	–	RSVD	No Connect	–	–
2	JT5	193	–	GND	GND	–	GND
2	JT5	194	–	RSVD	No Connect	–	–
2	JT5	195	35	ARTIX2_VCCO_35	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	196	35	ARTIX2_VCCO_35	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	197	–	RSVD	No connect	–	–
2	JT5	198	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	199	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	200	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	201	–	RSVD	No connect	–	–
2	JT5	202	–	RSVD	No connect	–	–
2	JT5	203	–	GND	GND	–	GND
2	JT5	204	36	ARTIX2_DUT_IO_196	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	205	36	ARTIX2_DUT_IO_181	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	206	35	ARTIX2_DUT_IO_186	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	207	–	GND	GND	–	GND
2	JT5	208	–	PWR_RESET_B	Power sequence complete	Output	CMOS - 3.3v

2	JT5	209	–	GND	GND	–	GND
2	JT5	210	34	ARTIX2_DUT_IO_25	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	211	34	ARTIX2_DUT_IO_26	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	212	36	ARTIX2_DUT_IO_27	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	213	34	ARTIX2_DUT_IO_28	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	214	34	ARTIX2_DUT_IO_29	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	215	–	GND	GND	–	GND
2	JT5	216	35	ARTIX2_DUT_IO_75	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	217	36	ARTIX2_DUT_IO_76	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	218	36	ARTIX2_DUT_IO_77	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	219	36	ARTIX2_DUT_IO_78	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	220	36	ARTIX2_DUT_IO_79	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	221	–	GND	GND	–	GND

2	JT5	222	34	ARTIX2_DUT_IO_125	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	223	34	ARTIX2_DUT_IO_126	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	224	15	ARTIX2_DUT_IO_127	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	225	15	ARTIX2_DUT_IO_128	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	226	15	ARTIX2_DUT_IO_129	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	227	–	GND	GND	–	GND
2	JT5	228	15	ARTIX2_DUT_IO_175	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	229	15	ARTIX2_DUT_IO_176	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	230	15	ARTIX2_DUT_IO_177	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	231	–	GND	GND	–	GND
2	JT5	232	–	RSVD	No Connect	–	–
2	JT5	233	–	GND	GND	–	GND
2	JT5	234	–	RSVD	No Connect	–	–
2	JT5	235	35	ARTIX2_VCCO_35	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	236	35	ARTIX2_VCCO_35	DUT I/O VCCO Power	Input	Power In - I/O Standard

2	JT5	237	–	RSVD	No connect	–	–
2	JT5	238	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	239	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	240	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	241	–	RSVD	No connect	–	–
2	JT5	242	–	GND	GND	–	GND
2	JT5	243	35	ARTIX2_DUT_IO_180	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	244	34	ARTIX2_DUT_IO_185	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	245	36	ARTIX2_DUT_IO_191	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	246	–	GND	GND	–	GND
2	JT5	247	–	PWR_ENABLE	Hard Reset	Output	Open-drain - pulled to PWR_DUT using 10k resistor
2	JT5	248	–	GND	GND	–	GND
2	JT5	249	–	GND	GND	–	GND
2	JT5	250	–	GND	GND	–	GND
2	JT5	251	–	GND	GND	–	GND
2	JT5	252	34	ARTIX2_DUT_IO_30	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	253	34	ARTIX2_DUT_IO_31	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	254	34	ARTIX2_DUT_IO_32	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	255	35	ARTIX2_DUT_IO_33	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	256	35	ARTIX2_DUT_IO_34	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	257	–	GND	GND	–	GND
2	JT5	258	35	ARTIX2_DUT_IO_80	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	259	34	ARTIX2_DUT_IO_81	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	260	35	ARTIX2_DUT_IO_82	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	261	34	ARTIX2_DUT_IO_83	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	262	34	ARTIX2_DUT_IO_84	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	263	–	GND	GND	–	GND
2	JT5	264	35	ARTIX2_DUT_IO_130	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	265	35	ARTIX2_DUT_IO_131	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	266	35	ARTIX2_DUT_IO_132	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	267	35	ARTIX2_DUT_IO_133	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	268	34	ARTIX2_DUT_IO_134	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	269	–	GND	GND	–	GND
2	JT5	270	–	GND	GND	–	GND
2	JT5	271	–	RSVD	No Connect	–	–
2	JT5	272	–	GND	GND	–	GND
2	JT5	273	–	GND	GND	–	GND
2	JT5	274	–	RSVD	No Connect	–	–
2	JT5	275	34	ARTIX2_VCCO_34	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	276	34	ARTIX2_VCCO_34	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	277	–	RSVD	No connect	–	–
2	JT5	278	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	279	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	280	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	281	–	RSVD	No connect	–	–
2	JT5	282	–	GND	GND	–	GND
2	JT5	283	34	ARTIX2_DUT_IO_190	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	284	34	ARTIX2_DUT_IO_195	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	285	–	RSVD	No connect	–	–
2	JT5	286	–	RSVD	No Connect	–	–
2	JT5	287	–	RSVD	No Connect	–	–
2	JT5	288	–	RSVD	No connect	–	–
2	JT5	289	–	GND	GND	–	GND
2	JT5	290	–	GND	GND	–	GND
2	JT5	291	–	GND	GND	–	GND
2	JT5	292	34	ARTIX2_DUT_IO_35	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	293	34	ARTIX2_DUT_IO_36	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	294	35	ARTIX2_DUT_IO_37	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	295	35	ARTIX2_DUT_IO_38	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	296	35	ARTIX2_DUT_IO_39	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	297	–	GND	GND	–	GND
2	JT5	298	34	ARTIX2_DUT_IO_85	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	299	35	ARTIX2_DUT_IO_86	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	300	35	ARTIX2_DUT_IO_87	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	301	34	ARTIX2_DUT_IO_88	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	302	34	ARTIX2_DUT_IO_89	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	303	–	GND	GND	–	GND
2	JT5	304	35	ARTIX2_DUT_IO_135	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	305	35	ARTIX2_DUT_IO_136	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	306	35	ARTIX2_DUT_IO_137	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	307	35	ARTIX2_DUT_IO_138	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	308	34	ARTIX2_DUT_IO_139	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	309	–	GND	GND	–	GND
2	JT5	310	–	GND	GND	–	GND
2	JT5	311	–	RSVD	No Connect	–	–
2	JT5	312	–	GND	GND	–	GND
2	JT5	313	–	GND	GND	–	GND
2	JT5	314	–	RSVD	No Connect	–	–
2	JT5	315	34	ARTIX2_VCCO_34	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	316	34	ARTIX2_VCCO_34	DUT I/O VCCO Power	Input	Power In - I/O Standard

2	JT5	317	–	RSVD	No connect	–	–
2	JT5	318	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	319	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	320	–	PWR_DUT	DUT board power input	Input	12V-17V
2	JT5	321	–	GND	GND	–	GND
2	JT5	322	–	GND	GND	–	GND
2	JT5	323	36	ARTIX2_DUT_IO_169	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	324	34	ARTIX2_DUT_IO_174	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	325	34	ARTIX2_DUT_IO_179	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	326	–	RSVD	No connect	–	–
2	JT5	327	–	RSVD	No connect	–	–
2	JT5	328	–	RSVD	No Connect	–	–
2	JT5	329	–	GND	GND	–	GND
2	JT5	330	–	GND	GND	–	GND
2	JT5	331	–	GND	GND	–	GND
2	JT5	332	34	ARTIX2_DUT_IO_40	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	333	34	ARTIX2_DUT_IO_41	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	334	34	ARTIX2_DUT_IO_42	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	335	34	ARTIX2_DUT_IO_43	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	336	34	ARTIX2_DUT_IO_44	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	337	–	GND	GND	–	GND
2	JT5	338	34	ARTIX2_DUT_IO_90	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	339	34	ARTIX2_DUT_IO_91	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	340	34	ARTIX2_DUT_IO_92	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	341	35	ARTIX2_DUT_IO_93	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	342	35	ARTIX2_DUT_IO_94	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	343	–	GND	GND	–	GND
2	JT5	344	34	ARTIX2_DUT_IO_140	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	345	35	ARTIX2_DUT_IO_141	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	346	35	ARTIX2_DUT_IO_142	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	347	35	ARTIX2_DUT_IO_143	DUT I/O	Bidir	CMOS/TTL - I/O Standard

2	JT5	348	35	ARTIX2_DUT_IO_144	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	349	–	GND	GND	–	GND
2	JT5	350	–	RSVD	No Connect	–	–
2	JT5	351	–	GND	GND	–	GND
2	JT5	352	–	RSVD	No Connect	–	–
2	JT5	353	–	GND	GND	–	GND
2	JT5	354	–	RSVD	No Connect	–	–
2	JT5	355	15	ARTIX2_VCCO_15	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	356	15	ARTIX2_VCCO_15	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	357	–	RSVD	No Connect	–	–
2	JT5	358	–	RSVD	No Connect	–	–
2	JT5	359	–	RSVD	No Connect	–	–
2	JT5	360	–	RSVD	No Connect	–	–
2	JT5	361	–	RSVD	No connect	–	–
2	JT5	362	–	RSVD	No connect	–	–
2	JT5	363	–	RSVD	No connect	–	–
2	JT5	364	34	ARTIX2_DUT_IO_173	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	365	34	ARTIX2_DUT_IO_178	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	366	–	RSVD	No connect	–	–
2	JT5	367	–	RSVD	No connect	–	–
2	JT5	368	–	RSVD	No connect	–	–

2	JT5	369	–	GND	GND	–	GND
2	JT5	370	–	GND	GND	–	GND
2	JT5	371	–	GND	GND	–	GND
2	JT5	372	34	ARTIX2_DUT_IO_45	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	373	34	ARTIX2_DUT_IO_46	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	374	34	ARTIX2_DUT_IO_47	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	375	34	ARTIX2_DUT_IO_48	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	376	34	ARTIX2_DUT_IO_49	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	377	–	GND	GND	–	GND
2	JT5	378	34	ARTIX2_DUT_IO_95	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	379	34	ARTIX2_DUT_IO_96	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	380	34	ARTIX2_DUT_IO_97	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	381	35	ARTIX2_DUT_IO_98	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	382	34	ARTIX2_DUT_IO_99	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	383	–	GND	GND	–	GND

2	JT5	384	35	ARTIX2_DUT_IO_145	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	385	35	ARTIX2_DUT_IO_146	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	386	35	ARTIX2_DUT_IO_147	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	387	35	ARTIX2_DUT_IO_148	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	388	35	ARTIX2_DUT_IO_149	DUT I/O	Bidir	CMOS/TTL - I/O Standard
2	JT5	389	–	GND	GND	–	GND
2	JT5	390	–	RSVD	No Connect	–	–
2	JT5	391	–	GND	GND	–	GND
2	JT5	392	–	RSVD	No Connect	–	–
2	JT5	393	–	GND	GND	–	GND
2	JT5	394	–	RSVD	No Connect	–	–
2	JT5	395	15	ARTIX2_VCCO_15	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	396	15	ARTIX2_VCCO_15	DUT I/O VCCO Power	Input	Power In - I/O Standard
2	JT5	397	–	RSVD	No Connect	–	–
2	JT5	398	–	RSVD	No Connect	–	–
2	JT5	399	–	RSVD	No Connect	–	–
2	JT5	400	–	RSVD	No Connect	–	–

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